Common Management Interface Specification

for

8X/16X PLUGGABLE TRANSCEIVERS

Rev 3.0 September 18, 2018

Abstract: This document defines the Common Management Interface Specification (CMIS)for pluggable modules such as QSFP Double Density (QSFP-DD), OSFP and COBO. This document provides a common specification for systems manufacturers, system integrators, and suppliers of modules and transceivers.

POINTS OF CONTACT:

Tom Palkert	Mark Nowell	Scott Sommers
Technical Editor	Co-Chair	Co-Chair
Molex	Cisco	Molex
2222 Wellington Court	170 West Tasman Dr	2222 Wellington Court
Lisle, IL 60532-1682	San Jose, CA 95134	Lisle, IL 60532-1682
Ph: +1 (952)-200-8542	Ph: +1 (613)-254-3391	Ph: +1 (630)-527-4317
tom.palkert at molex.com	mnowell at cisco.com	scott.sommers at molex.com

Change History:

Revision	Date	Changes
1.0	June 2017	First public release
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3.0	September 18	CMIS public release

Foreword

The development work on this specification was done by the QSFP-DD, OSFP and COBO advisory group. Further revisions of the CMIS shall be backwards compatible to Revision 3.0.

CONTENTS

1 Management Interface

1.1 Introduction

This specification defines the Common Management Interface Specification (CMIS) for QSFP-DD, OSFP and COBO in order to enable flexible use of modules and cable assemblies (hereafter referred to as modules unless cable assemblies are specifically mentioned) by the user. It shares some similarities with the management interfaces used in other form factors such as QSFP, SFP, and CFP. This specification supports a module with 8 host electrical lanes. Support for modules with more host lanes is possible (in increments of up to 8 lanes) by a bank selection feature (which allows several instances of an

adressable page to exist in the paged register map). Due to this new mechanism this specification is not backwards compatible with SFF-8636. Some host ports may support both 4-channel and 8-channel devices; when a 4-channel device is inserted into such a port the appropriate memory map (e.g. SFF-8636) must be used. This case is outside the scope of this document.

The host-to-module interactions needed to initialize active modules are presented in two state machines. A module-level state machine defines the initialization of the management interface as well as control of the module-wide power mode. A data path-specific state machine defines the host and module interactions and behaviors needed for power up and initialization of the data path(s) in the module.

The CMIS is intended to cover a wide range of possible module functionalities and applications, ranging from cable assemblies to coherent DWDM modules. The CMIS is designed with the intent not to burden the simple cases but to provide a common set of management interactions and a common register map.

In some modules, multiplexing of the high speed signals between the host electrical interface and the module media interface may occur in the module. In this specification, all references to lane numbers are based on the electrical connector interface lanes, unless otherwise indicated. In cases where a status or control aspect is applicable only to lanes after multiplexing or demultiplexing has occurred, the status or control is intended to apply to all lanes in the data path, unless otherwise indicated. Symmetry is expected between the Tx and the Rx hardware structure; for example Tx lanes that are multiplexed in the Tx are demultiplexed in the Rx. Each Application selected by the host is applied to the same Tx and Rx host electrical lanes.

1.2 Definitions and Acronyms

ACK: Acknowledge

ASCII: American Standard Code for Information Interchange: the numerical representation of a character

CDR: clock and data recovery

Checksum: a number derived from a block of digital data for the purpose of detecting errors.

CLEI: (Common Language Equipment Identification) code is a 10-byte field that contains the vendor’s CLEI code in ASCII characters (see www.commonlanguage.com)

Custom: Custom fields and formats are defined by the module manufacturer and may be unique to a specific vendor.

Data Path: Host electrical and module media lanes grouped together into a logical concept. A data path is intended to represent a group of lanes that will be powered up or down and initialized together.

DFB: Distributed Feedback Laser

DWDM: Dense Wavelength Division Multiplexing

EML: Externally Modulated Laser

Flat Memory: Single 256-byte memory implemented without paging

FP: Fabry-Perot Laser

NACK: Not Acknowledge

NV: Non-Volatile memory: a type of memory that can retrieve stored information even after having been power cycled

OM2: cabled optical fiber containing 50/125 um multimode fiber with a minimum overfilled launch bandwidth of 500 MHz-km at 850 nm and 500 MHz-km at 1300 nm as IEC 60793-2-10 Type A1a.1 fiber.

OM3: cabled optical fiber containing 50/125 um laser optimized multimode fiber with a minimum overfilled launch bandwidth of 1500 MHz-km at 850 nm and 500 MHz-km at 1300 nm as well as an effective laser launch bandwidth of 2000 MHz-km at 850 nm in accordance with IEC 60793-2-10 Type A1a.2 fiber.

OM4: cabled optical fiber containing 50/125 um laser optimized multimode fiber with a minimum overfilled launch bandwidth of 3500 MHz-km at 850 nm and 500 MHz-km at 1300 nm as well as an effective laser launch bandwidth of 4700 MHz-km at 850 nm in accordance with IEC 60793-2-10 Type A1a.3 fiber.

OM5: cabled optical fiber containing 50/125 um laser optimized multimode fiber with a minimum overfilled launch bandwidth of 3500 MHz-km at 850 nm, 1850 MHz-km at 953 nm and 500 MHz-km at 1300 nm as well as an effective laser launch bandwidth of 4700 MHz-km at 850 nm and 2470 MHz-km at 953 nm in accordance with IEC 60793-2-10 Type A1a.4 fiber.

OMA: Optical Modulation Amplitude: The difference between two optical power levels, of a digital signal generated by an optical source, *e.g.,* a laser diode.

OSNR: Optical Signal to Noise Ratio: The ratio between the optical signal power and the noise power in a given bandwidth.

OUI: Organizationally Unique Identifier: A unique vendor code assigned by the IEEE

Pave: Average Power: The average optical power

Post-cursor equalization: Rx output means used to reduce post-cursor ISI

Pre-cursor equalization: Rx output means used to reduce pre-cursor ISI

Pulse Amplitude Modulation, four levels (PAM4): a modulation scheme where two bits are mapped into four signal amplitude levels to enable transmission of two bits per symbol.

Rx: an electronic component (Rx) that converts an input signal (optical or electrical) to an electrical (retimed or non-retimed) output signal.

SDA: bidirectional Serial Data line

SCL: bidirectional Serial Clock line

SNR: Signal to Noise Ratio: The ratio of signal power to the noise power, expressed in decibels

TEC: Thermal Electric Cooler

TWI: Two Wire Interface

tWR: Time required to complete a single or sequential write to non-volatile memory.

Tx: a circuit (Tx) that converts an electricalinput signal to a signal suitable for the communications media (optical or electrical).

VCSEL: Vertical Cavity Surface Emitting Laser

WDM: Wavelength Division Multiplexing

1.3 Management Interface Timing Specifications and Protocol

1.3.1 Introduction

The management interface between Host and Module consists of a serial communications interface and small set of discrete hardware signals described in Appendix A – Form Factor Signal Names. The communication interface allows the Host to access registers in the Module. It is described in detail in the remainder of this section.

Communication between Host and Module is done via a Two Wire serial Interface(TWI). Detailed electrical specifications and TWI timing are given in the appropriate hardware/module specification.

1.3.2 Management Interface Timing Specification

The management interface timing requirements are defined in the appropriate hardware specification. The TWI address of the module is 1010000X (A0h). The host shall initially address the module using a 0-400 kHz SCL clock speed. If a higher management interface speed is supported, (See Table 18) the host may switch to the 0-1MHz SCL clock speed.

In order to allow access to multiple modules on the same TWI bus, some form factors include and require the module to support a module select signal, (ModSelL). For these form factors, before initiating a TWI bus communication, the host shall provide setup time on the ModSelL line of all modules on the TWI bus. The host shall not change the ModSelL line of any module until the TWI bus communication is complete and the hold time requirement is satisfied.

1.3.3 Signal Interface

The TWI shall consist of a master and slave. The host shall be the master and the module shall be the slave. Control and data are transferred serially. The master shall initiate all data transfers. Data can be transferred from the master to the slave and from the slave to the master. The TWI shall consist of clock (SCL) and data (SDA) signals.
The master utilizes SCL to clock data and control information on the TWI bus. The master and slave shall latch the state of SDA on the positive transitioning edge of SCL.
The SDA signal is bi-directional. During data transfer, the SDA signal shall transition when SCL is low. A transition on the SDA signal while SCL is high shall indicate a stop or start condition.

1.3.4 Serial Interface Protocol

1.3.4.1 Operational States and State Transition

1.3.4.1.1 Start

A high-to-low transition of SDA with SCL high is a START condition. All TWI bus operations shall begin with a START condition.

1.3.4.1.2 Stop

A low-to-high transition of SDA with SCL high is a STOP condition. All TWI bus operations shall end with a STOP condition

1.3.4.1.3 Acknowledge

After sending each 8-bit word, the side driving the TWI bus releases the SDA line for one bit time, during which the monitoring side of the TWI bus is allowed to pull SDA low (zero) to acknowledge (ACK) that it has received each word. Write data operations shall be acknowledged by the slave for all bytes. Read data operations shall be acknowledged by the master for all but the final byte read, for which the master shall respond with a non-acknowledge (NACK) by permitting SDA to remain high and followed by a STOP.

1.3.4.1.4 Clock Stretching

To extend the TWI data transfer the slave asserts clock low. This should be initiated while the clock is low. This can be used by the slave to delay completion of the operation.

1.3.4.2 Reset TWI

1.3.4.2.1 Power On Reset

The interface shall enter a reset state upon application of power.

1.3.4.2.2 TWI Protocol Reset

Synchronization issues may cause the master and slave to disagree on the specific bit location currently being transferred, the type of operation or even if an operation is in progress. The TWI protocol has no explicitly defined reset mechanism. The following procedure may force completion of the current operation and cause the slave to release SDA.

a) The master shall provide up to nine SCL clock cycle (drive low, then high) to the slave
b) The master shall monitor SDA while SCL is high on each cycle.
c) If the slave releases SDA, it will be high and the master is then free to initiate a START operation for the next transaction
d) If SDA remains low after a full nine clock cycles the TWI protocol reset has failed

1.3.4.2.3 Reset Signal

Some implementations may include a reset signal. If provided, upon assertion of the reset signal the TWI shall transition to the reset state.

1.3.4.3 TWI Binary Frame Format

1.3.4.3.1 Read/Write Controls

After the start condition, the first 8-bit word of a TWI bus operation shall consist of '1010000' followed by a read/write control bit.
The least significant bit indicates if the operation is a data read or write. A read operation is performed if this bit is high and a write operation is executed if this bit is set low. Upon completion of the control word transmission the slave shall assert the SDA signal low to acknowledge delivery (ACK) of the control/address word.

1.3.4.3.2 Address and Data

Following the read/write control bit, addresses and data words are transmitted in 8-bit words. Data is transferred with the most significant bit (MSB) first. Multiple Byte transactions shall be transmitted in increasing byte address order over the TWI.

1.3.5 Read/Write Operations

1.3.5.1 Slave Memory Address Counter (Read and Write Operations)

All TWI slaves maintain an internal data word address counter containing the last address accessed during the latest read or write operation, incremented by one. The address counter is incremented whenever a data word is received or sent by the slave. This

address remains valid between operations as long as power to the slave is maintained. Upon loss of power to or reset of the module or upon transactions not terminated by a Stop condition, the slave address counter contents may be indeterminate. The address roll-over during read and writes operations is from the last byte of the 128-byte memory page to the first byte of the same page.

The host shall use single 2-byte reads to retrieve all 16-bit data, to guarantee data coherency. The module shall prevent the host from acquiring partially updated multi-byte data during a 2-byte read. Data consistency for accesses to more than two bytes requires an application level interaction protocol using fields in the register map. It is not guaranteed by the basic R/W interaction primitives.

1.3.5.2 Read Operations

1.3.5.2.1 Current Address Read

A current address read operation requires only the slave address read word (10100001) be sent. Once acknowledged by the slave, the current address data word is serially clocked out. The transfer is terminated when the master responds with a NACK and a STOP instead of an acknowledge.

		<--- CONTROL WORD --->																		
MASTER	START	MSB						LSB	READ									NACK	STOP
		1	0	1	0	0	0	0	1	0	x	x	x	x	x	x	x	x	1	
SLAVE										ACK	MSB							LSB		
											<---- DATA WORD ----->									

Figure 1: Module Current Address Read Operation

1.3.5.2.2 Random Read

A random read operation requires a dummy write operation to load in the target byte address. This is accomplished by the following sequence: The target 8-bit data word address is sent following the device address write word (10100000) and acknowledged by the slave. The master then generates another START condition (aborting the dummy write without incrementing the counter) and a current address read by sending a device read address (10100001). The slave acknowledges the device address and serially clocks out the requested data word. The transfer is terminated when the master responds with a NACK and a STOP instead of an acknowledge.

		<--CONTROL WORD -->									<BYTE OFFSET ADDRESS>								
MASTER	START	MSB						LSB	WRITE		MSB							LSB	
		1	0	1	0	0	0	0	0	0	x	x	x	x	x	x	x	x	0
SLAVE										ACK									ACK

	<- CONTROL WORD -->																		
START	MSB						LSB	READ										NACK	STOP
	1	0	1	0	0	0	0	1	0	x	x	x	x	x	x	x	x	1	
									ACK	MSB							LSB		
										<---- DATA WORD n---->									

Figure 2: Module Random Read

1.3.5.3 Sequential Read

Sequential reads are initiated by either a current address read (see Figure 3) or a random address read (see Figure 4). To specify a sequential read, the host responds with an acknowledge (instead of a STOP) after each data word. As long as the module receives an acknowledge, it shall serially clock out sequential data words. The sequence is terminated when the host responds with a NACK and a STOP instead of an acknowledge.

		<- CONTROL WORD -->																
MASTER	START	MSB						LSB	READ									ACK
		1	0	1	0	0	0	0	1	0	x	x	x	x	x	x	x	x	0
SLAVE										ACK	MSB							LSB	
											<---- DATA WORD n---->								

								ACK									NACK	STOP
x	x	x	x	x	x	x	x	0	x	x	x	x	x	x	x	x	1	
MSB							LSB		MSB							LSB		
<-- DATA WORD n+1 --->									<-- DATA WORD n+x --->									

Figure 3: Sequential Address Read Starting at Module Current Address

1.3.5.3.1 Sequential Read from Random Start Address

		<- CONTROL WORD -->									<BYTE OFFSET ADDRESS>								
MASTER	START	MSB						LSB	WRITE		MSB							LSB	
		1	0	1	0	0	0	0	0	0	x	x	x	x	x	x	x	x	0
SLAVE										ACK									ACK

	<- CONTROL WORD -->																
START	MSB						LSB	READ									ACK
	1	0	1	0	0	0	0	1	0	x	x	x	x	x	x	x	x	0
									ACK	MSB							LSB	
										<---- DATA WORD n---->								

								ACK									NACK	STOP
x	x	x	x	x	x	x	x	0	x	x	x	x	x	x	x	x	1	
MSB							LSB		MSB							LSB		
<-- DATA WORD n+1 --->									<-- DATA WORD n+x --->									

Figure 4: Sequential Address Read Starting with Random Module Read

1.3.5.4 Write Operations

A write operation requires an 8-bit data word address following the device address write word (10100000) and acknowledgement. Upon receipt of this address, the slave shall again respond with a zero (ACK) to acknowledge and then clock in the first 8-bit data word. Following the receipt of the 8-bit data word, the slave shall output a zero (ACK) and the master must terminate the write sequence with a STOP condition for the write cycle to begin. If a START condition is sent in place of a STOP condition (i.e. a repeated START per the TWI specification) the write is aborted and the data received during that operation is discarded. Upon receipt of the proper STOP condition, the slave enters an internally timed write cycle, tWR, to internal memory. (See appropriate Hardware specification for tWR timing) The slave disables its management interface input during this write cycle and shall not respond or acknowledge subsequent commands until the internal memory write is complete. Note that TWI 'Combined Format' using repeated START conditions is not supported on write commands.

		<- CONTROL WORD -->									<BYTE OFFSET ADDRESS>									<- DATA WORD ->									
MASTER	START	MSB						LSB	WRITE		MSB							LSB		MSB							LSB		STOP
		1	0	1	0	0	0	0	0	0	x	x	x	X	x	x	x	x	0	x	x	x	x	x	x	x	x	0	
SLAVE										ACK									ACK									ACK	

Figure 5: Module Write Byte Operation

1.3.5.4.1 Sequential Write

The TWI slave shall support a sequential byte write of up to eight bytes without repeatedly sending slave address and memory address information. In a sequential write, the host should not include in the sequence a mixture of volatile and non-volatile registers. It should be noted that at the end of each 128 byte page, the next address rolls over to the first byte of the same page.

A sequential write is initiated the same way as a single byte write, but the host master does not send a stop condition after the first word is clocked in. Instead, after the slave acknowledges receipt of the first data word, the master can transmit additional data words: seven additional words for non-volatile memory and volatile memory. The slave shall send an acknowledge after each data word received. The slave may act on write data after generating the acknowledge or it may buffer the write transaction.

The master must terminate the sequential write sequence with a STOP condition. Upon receipt of the proper Stop condition, for writes to non-volatile memory, the slave may enter an internally timed write cycle, tWR, to internal memory. The slave may disable its management interface input during this write cycle and may not respond or acknowledge subsequent commands until the internal memory write is complete. If there is no proper STOP condition, the results of the sequential write are unpredictable.

Note that TWI 'combined format' using repeated START conditions is not supported on write commands.

		<- CONTROL WORD -->									<BYTE OFFSET ADDRESS>								
MASTER	START	MSB						LSB	WRITE		MSB							LSB	
		1	0	1	0	0	0	0	0	0	x	x	x	x	x	x	x	x	0
SLAVE										ACK									ACK

MSB							LSB		MSB							LSB			
x	x	x	x	x	x	x	x	0	x	x	x	x	X	x	x	x	0		
								ACK									ACK		
<--- DATA WORD n --->									<--- DATA WORD n+1--->										

MSB							LSB		MSB							LSB				STOP
x	x	x	x	x	x	x	x	0	x	x	x	x	x	x	x	x	0			
								ACK									ACK			
<--- DATA WORD n+2--->									<--- DATA WORD n+x--->											

Figure 6: Module Sequential Write Operation

1.3.5.4.2 Acknowledge Polling

Once the module internally timed write cycle has begun (and inputs are being ignored on the bus) acknowledge polling can be used to determine when the write operation is complete. This involves sending a START condition followed by the device address word. Only if the internal write cycle is complete shall the module respond with an acknowledge to subsequent commands, indicating read or write operations can continue.

1.3.6 Timing for Soft Control and Status Functions

Timing for module soft control, status functions, and squelch and disable timings can be found in the appropriate Module Hardware Specification.

1.4 Module State Machine

The purpose of the Module State Machine is twofold: to provide both a description of the bring-up process for the management interface as well as to identify the module-wide power mode. The State Machine is engaged after module insertion and power on. The Module State Machine is applicable to both modules and cable assemblies, whether passive or active and is pictured in Figure 7. This common management interface specification is designed to be applied to multiple form factors. Therefore, actions and properties are described using generic terms instead of using application-specific signal names. Refer to Appendix A – Form Factor Signal Names for the association between generic descriptors in this section and application-specific signal names.

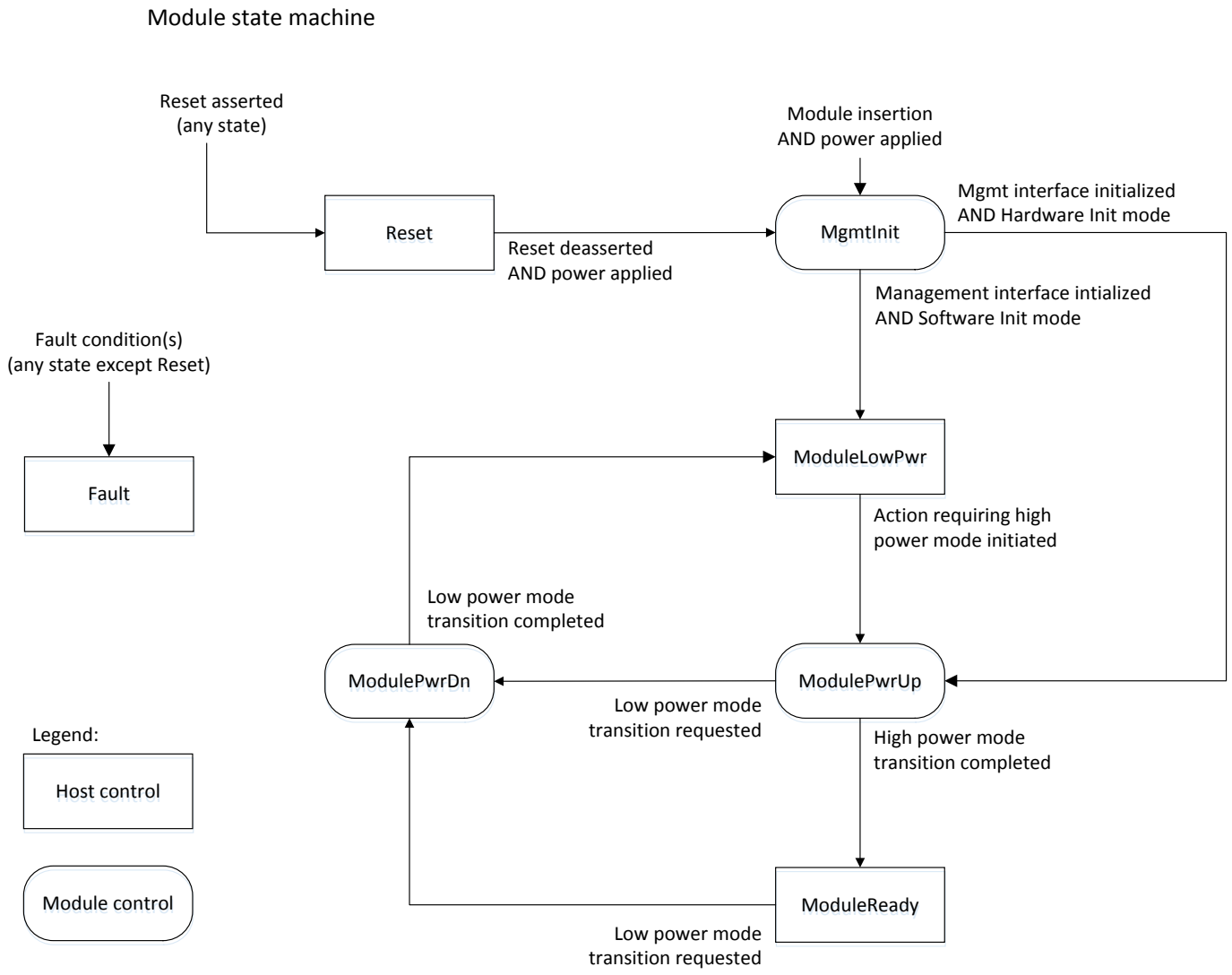

Figure 7: Module State Machine

The Module State Machine describes module-wide behaviors and properties. For data path-specific behaviors and properties, refer to the Data Path State Machine in Section 1.5.3.

States with a rectangular outline are host control states, where the module is waiting for host-initiated actions, either through the memory map or through a hardware signal. The duration of host control states is unbounded.

States with an oval outline are transient states where the module is in control of initialization activities. These module control states have an implementation-dependent duration. Dynamic register content is unreliable during module control states.

Table 1 and Table 2 provide a summary of the high-level behaviors and properties of each module state for passive copper cable assembly and active module implementations, respectively. Implementers of passive copper cable assemblies should note that this specification was designed to allow for flat-memory EEPROM implementations for that cable type. Active modules and active cable assemblies shall use the paged memory model. For all module types, refer to sections 1.4.3-1.4.9 for detailed requirements for each state.

Table 1- Passive copper cable assembly state behaviors

State	**Power Mode**	**Behavior in state**	**Exit condition**	**Next state**	**Required/ Optional**
Reset	Low Power	Management interface in reset	Reset signal deasserted and power applied	MgmtInit	Optional
MgmtInit	Low Power	Management interface powering up and initializing	Module Management Interface ready AND Interrupt signal asserted OR t_init timeout. (See Hardware Specification)	ModuleLowPwr	Required
			Reset signal asserted	Reset	
ModuleLowPwr	Low Power	Management interface available	Reset signal asserted	Reset	Required
ModulePwrUp		This state is not applicable to passive copper cable assemblies			
ModuleReady		This state is not applicable to passive copper cable assemblies			
ModulePwrDn		This state is not applicable to passive copper cable assemblies			
Fault		This state is not applicable to passive copper cable assemblies			

Table 2- Active module state behaviors

State	Power Mode	Behavior in state	Exit condition	Next state	Required/ Optional
Reset	Low Power	Management interface and all module electronics in reset	Reset signal deasserted and power applied	MgmtInit	Required
MgmtInit	Low Power	Management interface powering up and initializing	Software Init mode AND (Module Mgmt Interface ready OR t_init timeout) (See Hardware Specification)	ModuleLowPwr	Required
			Hardware Init mode AND (Module Mgmt Interface ready OR t_init timeout) (See Hardware Specification)	ModulePwrUp	
			Reset signal asserted	Reset	
			Fault condition detected	Fault	
ModuleLowPwr	Low Power	Management interface available, host may configure module	Host requests an action that requires High Power mode	ModulePwrUp	Required
			Reset signal asserted	Reset	
			Fault condition detected	Fault	
ModulePwrUp	High Power	Module transitioning to high power mode	Power up activities are complete	ModuleReady	Required
			Host requests module return to Low Power mode	ModulePwrDn	
			Reset signal asserted	Reset	
			Fault condition detected	Fault	
ModuleReady	High Power	Module may be consuming power up to the level defined in the fields in Table 30	Host requests module return to Low Power mode	ModulePwrDn	Required
			Reset signal asserted	Reset	
			Fault condition detected	Fault	
ModulePwrDn	High Power	Module transitioning to low power mode	Module has returned to Low Power mode	ModuleLowPwr	Required
			Reset signal asserted	Reset	
			Fault condition detected	Fault	
Fault	Low Power	Module is waiting for host action	Module power down	N/A	Optional
			Reset signal asserted	Reset	

Certain Module State Machine state transitions shall cause the Module State Changed flag to be set, while other transitions shall not set this flag. In general, module-initiated state transitions result in the Module State Changed flag being set. Table 3 below defines the appropriate flag behavior for each valid state transition.

Table 3- Module State Changed flag behaviors

Prior state	Next state	Causes Module State Changed flag to be set?
Reset	MgmtInit	No
Any state	Reset	No
Any state	Fault	Yes
MgmtInit	ModuleLowPwr	Yes
MgmtInit	ModulePwrUp	No
ModuleLowPwr	ModulePwrUp	No
ModulePwrUp	ModuleReady	Yes
ModulePwrUp	ModulePwrDn	No
ModuleReady	ModulePwrDn	No
ModulePwrDn	ModuleLowPwr	Yes

1.4.1 Module Init Modes

Under normal circumstances, modules are expected to power up into the ModuleLowPwr state, to allow host management software to configure the module properties prior to operation. This software-controlled power-up behavior is called Software Init mode in this specification. Some module form factors may provide an alternative Hardware Init mode (see Appendix A – Form Factor Signal Names), where the module proceeds to the ModulePwrUp state to power up the default Application(s) data path(s). The support of hardware input signal-selectable Init mode is form factor dependent, but is not required for this specification. When not implemented, the module shall power up according to Software Init mode procedures, as described in this document. The module shall only observe the state of the Init mode signal during the MgmtInit state. Any host changes to the Init mode signal that occur after MgmtInit will not be applied until the module is reset or power cycled. Init mode is not applicable to passive copper cable assemblies.

When booting in Hardware Init mode, the module shall utilize power-on defaults for all data path configuration settings, including Application Select.

1.4.2 Module Power Mode and Module and Data Path State Machine interactions

The module power mode may be used by the host to limit module power consumption to one of two thresholds – Low Power mode or High Power mode. When in Low Power mode, the maximum power consumption of the module must remain below a form factor defined maximum. Passive copper cable assemblies are in Low Power mode at all times and are fully functional. Active module functionality when in Low Power mode is limited to host-to-module interactions over the management interface. All modules shall initially power up in Low Power mode, unless booting in Hardware Init mode. When in High Power mode, active modules may be fully functional, depending on configuration settings, and the maximum power consumption of the module shall be limited to the advertised Module Power Class (Table 30).

The module power mode is dependent on the state of the data paths in the module. The Module State Machine reflects the module power mode, as shown in Table 1 and Table 2. As soon as data path power up is initiated on one or more data paths, the module shall transition to High Power mode. During this power up process, the Data Path State Machine is in the DataPathInit state and the Module State Machine is in ModulePwrUp. Once power up is complete on all requested lanes, the Data Path State Machine and Module State Machines shall transition to DataPathActivated and ModuleReady, respectively. Refer to the Data Path State Machine in Section 1.5.3 for details regarding Data Path State behaviors. Implementers should note that it is theoretically possible to create an active module whose maximum power dissipation is below the Low Power Mode threshold, even when fully functional. To maintain consistency for host firmware implementations, such

modules shall continue to follow the rules set forth in this section, requiring the host to explicitly request Data Path power up and down through the DataPathPwrUp bits and following the module state transitions initiated by host actions.

The maximum High Power mode power consumption for the module is identified by the module power advertising fields in Table 30. Once the module is in High Power mode, it shall remain in High Power mode until a Fault occurs or until explicitly directed by the host to transition to Low Power mode, by the host setting the ForceLowPwr bit in the memory map (Table 23) or asserting the LowPwr signal. Implementation of the LowPwr signal is optional and form factor dependent (see Appendix A – Form Factor Signal Names).

Module implementers should note that the host may request power up or power down of module data paths during normal operation but the module may remain in High Power mode, even if all data paths are powered down individually. The requirement of exclusive ForceLowPwr bit/LowPwr signal control for entry into Low Power mode is provided to allow faster re-power up of data paths than would be possible if the module returned to Low Power mode automatically when all data paths are returned to the "DataPathDeaactivated" state.

When the host requests a return to Low Power mode and the module state is in ModulePwrUp or ModuleReady, the Data Path State Machines for all data paths become dependent on the Module State Machine. The Module State Machine shall transition to ModulePwrDn and all Data Path State Machines that are not already in DataPathDeactivated shall transition to DataPathDeinit. This transition shall occur even if the module is booting in Hardware Init Mode or the Data Path state is in DataPathInit. When all data paths are powered down and the module has returned to Low Power mode, the Module State Machine and Data Path State Machines shall transition to ModuleLowPwr and DataPathDeactivated, respectively.

If the host requests a transition to Low Power Mode while the module is already in Low Power Mode, the module shall remain in Low Power Mode until this request is cleared. If the module is booting in Hardware Init Mode and the host sets the ForceLowPwr bit or asserts the LowPwr signal during MgmtInit, the module shall follow the initialization activities associated with Software Init Mode.

1.4.3 Reset State

A low level on the Reset signal for longer than the minimum reset pulse length initiates a complete module reset. Refer to form factor-specific documentation for the minimum reset pulse duration. A reset can also be initiated through software using the Software Reset bit (Table 23). A software reset can only trigger a transient reset after which the module will enter MgmtInit. The Reset state shall be entered from any state by assertion of the Reset signal. The shutdown procedure used by the module for a reset event is implementation dependent.

For passive copper cables, assertion of the Reset signal may optionally hold the EEPROM in reset, however the data path shall remain active. When an active module enters the Reset state, all Data Path States shall transition immediately to the DataPathDeactivated state. Refer to section 1.5.3 for Data Path State behaviors. All lasers and module electronics shall be placed in reset upon entry into the reset state for the duration of the state.

The module shall remain in Low Power mode throughout the Reset state. All interrupts shall be suppressed while the module is in the Reset state.

Management interface transactions initiated by the host during the Reset state may be ignored by the module. Note: While the Reset signal is asserted, the management interface may be held in reset and may not respond (NAK).

After de-assertion of the Reset signal, the module may not respond until the MgmtInit state is complete. The Reset state can only be exited by deassertion of the Reset signal and application of power. Upon exit from the Reset state, the module shall enter the MgmtInit state.

1.4.4 MgmtInit State

The MgmtInit state is a module control state that is entered any time the module is brought out of the Reset state, (either hardware or software reset). The MgmtInit state is applicable to both active modules and passive copper cable assemblies.

During this state, the module shall configure the memory map and initialize the management interface for access by the host. The module may perform limited power-up of the high-speed data path circuitry, however the module shall remain in Low Power Mode throughout this state. For active modules, all Data Path States shall remain in DataPathDeactivated throughout MgmtInit. The module may ignore all TWI transactions while in the MgmtInit state.

Interrupt flag conformance in the MgmtInit state is defined in Section 1.6.1. All disallowed interrupt flags shall not be set during MgmtInit.

Before the module exits the MgmtInit state, all memory map register locations shall be set to their power-on defaults. In Hardware Init mode, power-up defaults may include DataPathPwrUp bits. The module shall have completed MgmtInit within the module form-factor dependent management interface initialization time, defined as the time from power on (defined as the instant when supply voltages reach and remain at or above the minimum level specified in the form factor-dependent specification), hot plug, or the rising edge of the Reset signal until the module has configured the memory map to default conditions and activated the management interface.

Upon completion of MgmtInit, the next state depends on the Init mode of the module. If the module is booting in Software Init mode, the next state is ModuleLowPwr. If the module is booting in Hardware Init mode, the next state is ModulePwrUp.

1.4.5 ModuleLowPwr State

The ModuleLowPwr state is a host control state, where the management interface is fully initialized and operational and the device is in Low Power mode. During this state, the host may configure the module using the management interface and memory map. Some examples of configuration activities include reading the ID and device property fields, setting CDR and other lane attributes and configuration of monitor masks. Details of host-module interactions in the ModuleLowPwr state are implementation dependent and are outside the scope of this specification.

Upon entry into the ModuleLowPwr state, the module shall set the Module State register (Table 18) to the ModuleLowPwr state and set the Module State Changed interrupt flag (Table 21). The module shall not clear any interrupt flags on the state change. Interrupt flags are only cleared when the host reads the flag. Host implementers should note that the host must clear the ForceLowPwr bit (if set) (Table 23) before setting DataPathPwrUp to exit the ModuleLowPwr state (Table 53).

Interrupt flag conformance in the ModuleLowPwr state is defined in Section 1.6.1. All disallowed interrupt flags shall not be set during ModuleLowPwr.

When the host has completed module configuration, the host may initialize one or more data paths by setting the applicable bits in the DataPathPwrUp register (Table 53) in the

memory map. Refer to the Data Path State Machine section 1.5.3 for data path control and attribute details.

As soon as the host sets any bit in the DataPathPwrUp register, the module state shall transition to ModulePwrUp. Implementers should note that modules in ModuleLowPwr shall ignore the InitMode signal.

1.4.6 ModulePwrUp state

The ModulePwrUp state is a module control state used to inform the host that one or more data paths is in the process of powering up to full power operation.

Entry into ModulePwrUp can occur from ModuleLowPwr, when the host sets one or more of the DataPathPwrUp bits (Table 53), or from MgmtInit if the module is in Hardware Init mode. In ModulePwrUp the module advances the Data Path State Machines, where the associated DataPathPwrUp bits are 1, to DataPathInit. Implementers should note that modules in ModulePwrUp shall ignore the InitMode signal. Upon entry into ModulePwrUp, the module shall set the Module State register (Table 18) to the ModulePwrUp state.

The module may be in High Power mode at any time during the ModulePwrUp state.

Interrupt flag conformance in the ModulePwrUp state is defined in section 1.6.1. All disallowed interrupt flags shall not be set during ModulePwrUp. However, the module shall not clear any interrupt flags on the state change. Interrupt flags are only cleared when the host reads the flag.

When the associated data paths reach the DataPathActivated state, the module shall transition to the ModuleReady state.

If the host sets the ForceLowPwr bit (Table 23) or asserts the LowPwr signal while in ModulePwrUp, the module shall immediately transition to ModulePwrDn.

1.4.7 ModuleReady State

The ModuleReady state is a host control state that indicates that the module is in High Power mode. One or more data paths may be powered, but this is not a requirement for the module to be in ModuleReady.

Upon entry into the ModuleReady state, the module shall set the Module State register (Table 18) to the ModuleReady state and set the Module State Changed interrupt flag (Table 21). The module shall not clear any interrupt flags on the state change. Interrupt flags are only cleared when the host reads the flag.

Interrupt flag conformance in the ModuleReady state is defined in section 1.6.1. All disallowed interrupt flags shall not be set during ModuleReady.

While in ModuleReady, the host may power up or down individual or groups of data paths. The only non-Reset or Fault action that results in an exit from ModuleReady is if the host sets the ForceLowPwr bit (Table 23) or asserts the LowPwr signal. Either of these actions shall result in a Module state transition to ModulePwrDn. Implementers should note that modules in ModuleReady shall ignore the InitMode signal.

1.4.8 ModulePwrDn State

The ModulePwrDn state is a module control state that is used to inform the host that the module is in the process of returning to Low Power mode.

Upon entry into the ModulePwrDn state, the module shall set the Module State register (Table 18) to the ModulePwrDn state and transition all Data Path States to DataPathDeinit.

The module may be in High Power mode at any time during the ModulePwrDn state.

Interrupt flag conformance in the ModulePwrDn state is defined in section 1.6.1. All disallowed interrupt flags shall not be set during ModulePwrDn. However, the module shall not clear any interrupt flags on the state change. Interrupt flags are only cleared when the host reads the flag.

When all the data paths reach the DataPathDeactivated state and the module is in low power mode, the module shall transition to the ModuleLowPwr state. Implementers should note that modules in ModulePwrDn shall ignore the InitMode signal.

1.4.9 Fault State

The Fault state is provided for notification to the host that a module fault has occurred. Implementation of the Fault state is form factor dependent. The Fault state shall only be entered when module detects a condition (e.g. TEC runaway, flash corruption) that could cause damage. The module shall be in Low Power mode during the Fault state.

1.5 Application/Data Path Overview

This specification uses concepts of Applications and Data Paths to organize host interactions with the module.

The module uses Applications to advertise the set of industry standards that it supports. An Application is defined as a combination of an industry standard host electrical interface and an industry standard module media interface. A module may support multiple different Applications and/or multiple instances of the same Application.

The host selects one or more Applications from the advertised options. Each instance of an Application is referred to as a Data Path. Each Data Path is initialized, powered and controlled independently by the host.

A module may advertise support for a single Application. For example, a module advertises an Application that consists of a CAUI-4 host electrical interface and a 100GBASE-SR4 media interface combination. In this example, the module could advertise support for one or two instances of the Application. Each instance of the Application selected by the host would be a separate Data Path, where each Data Path includes four host electrical lanes and four module media lanes.

A module may also advertise support for multiple Applications. For example, a module advertises an Application that consists of a 400GAUI-8 host electrical interface and a 400GBASE-DR4 media interface combination, and a second Application that consists of a 100GAUI-2 host electrical interface and a 100GBASE-DR media interface combination. The host may select one instance of the first Application or up to four instances of the second Application. Each instance of each selected Application becomes a separate Data Path.

1.5.1 Host Electrical and Module Media Lane Background

The module provides a host electrical interface and a module media interface. The host electrical interface consists of the module transmitter input signals and receiver output signals. These signals are communicated over electrical differential pairs called host electrical lanes. The media interface consists of the module transmitter output signals

and receiver input signals. These signals are communicated over wires or a combination of physical fibers and wavelengths, all called module media lanes.

Associated with each interface is a set of registers to control and report status for these signals at that interface. All references to host electrical lanes or module media lanes in this document are referring to the respective registers that control or describe those signals.

An Application consists of one or more host electrical lanes and one or more module media lanes. The module advertises the lane or group of lanes onto which an instance of an Application can be assigned. The lane or group of lanes supported by the instance of the Application are identified by the lowest numbered lane in that instance. This identification is advertised for both the host electrical and module media interfaces. Within each instance of an Application, all lanes shall be numbered consecutively on both interfaces, starting with the advertised lowest lane number. Refer to Section 1.5.2 for details on Application advertising methodology.

For each Application where the module supports multiple Application instances, hosts need to be able to determine which host electrical lane group corresponds to which module media lane group for each possible Application instance in the module. Modules shall associate the Nth host electrical lane group of the Application with the Nth module media lane group for the same Application. This rule is best illustrated by means of an example. A module advertising support for four instances of a 100GAUI-2 to 100GBASE-DR Application must identify the lowest lane number for each instance on both interfaces. As shown in Figure 8 for this example, the Application can be assigned starting on host electrical lane 1, 3, 5, or 7. These possibilities are the first, second, third, and fourth lane groups. By rule, the first lane group on the media interface in this example, which starts at media lane 1, must correspond to the first lane group on the host interface, which starts on host lane 1. The second lane group on the media interface, which starts on media lane 2, must correspond to the second lane group on the host interface, which starts on host lane 3, and so on. Therefore, in this example, the module would advertise host electrical lanes 1, 3, 5, and 7 are supported as lowest numbered lanes for the Application, and module media lanes 1, 2, 3, and 4 are supported as the corresponding lowest numbered lanes on the media interface.

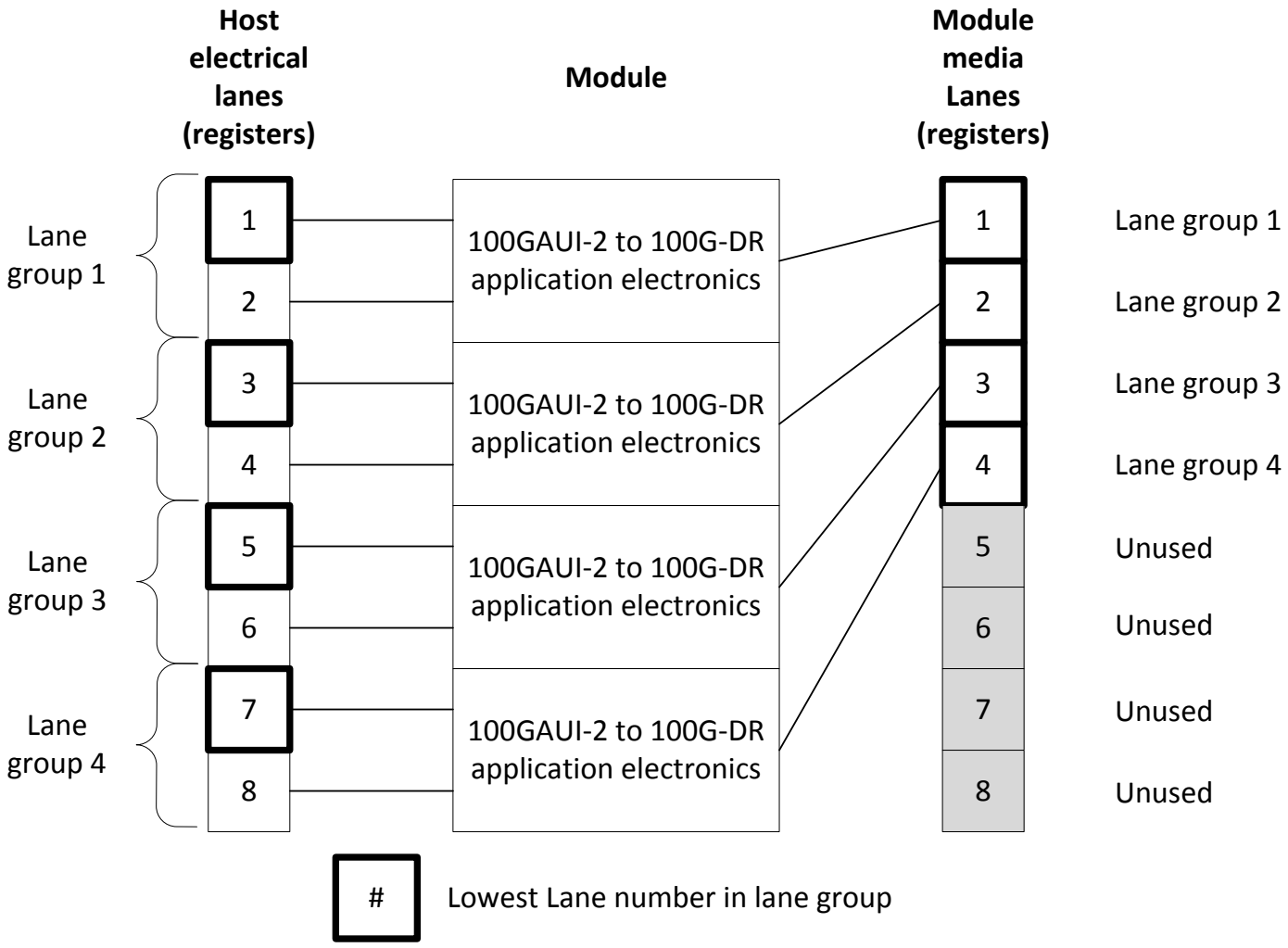

Figure 8: Lane Assignment Example

1.5.2 Application Advertising Methodology

An Application is defined by a combination of an industry standard specification for the host electrical interface and an industry standard specification for the module media interface. These standards define the signaling baud rate, the signaling modulation format and the number of lanes for the respective interface.

The module identifies supported Applications through an Application Advertising table. Within the table, each application is identified by a unique Application Select code (ApSel code), which the host will use to select the Application.

Table 4 below describes the contents of one entry in the Application Advertising Table, which corresponds to one ApSel code.

In the first byte, the Host Electrical Interface Code identifies the industry standard for the host electrical interface. The list of defined codes can be found in Appendix C Table 78. Table 78 identifies the host interface signaling rate, modulation format, and standard-defined lane count(s) for each Host Electrical Interface Code. The module defines the maximum supported host interface lane count in the Host Lane Count field,

described below. The first unused entry in the table shall be coded FFh to indicate the end of the list of supported Applications.

In the second byte, the Module Media Interface Code identifies the industry standard for the Module Media interface. The list of defined codes can be found in Appendix C Table 79 through Table 83. The module identifies which module media interface table applies to the module using the Module Type advertising field in Lower Page 00h Byte 85. The module media interface tables identify the media interface signaling rate, modulation format, and standard-defined lane count(s) for each Module Media Interface Code. The module defines the maximum supported media interface lane count in the Media Lane Count field, described below.

The third byte defines the number of lanes for the host electrical interface and the module media interface. The lane counts shall be consistent with the standards identified in the first and second bytes.

The fourth and fifth bytes identify the lanes where the Application is supported on the host and media interfaces, respectively. The module may support multiple instances of a given Application, so each Lane Assignment Options field identifies the lowest numbered lane in a consecutive group of lanes to which the Application can be assigned. For example, a module supporting two CAUI-4 Application instances that can be assigned to Host electrical interface lanes 1-4 and 5-8 would advertise a Host Lane Assignment Options value of 00010001b, to indicate that the lowest numbered lane for assignment of an instance of the CAUI-4 Application can be lane 1 or lane 5. The fifth byte (Media Lane Assignment Options) identifies where the Application instance is supported on the media interface. The Media Lane Assignment Options register is located on memory map page 01h in Table 47, separate from the first four bytes. The Media Lane Assignment Options register is not required for copper cable assemblies.

Table 4- Module Application Advertising format for one application

Byte	Bits	Name	Description
First	7-0	Host Electrical Interface Code	Code from Appendix C Table 78. The first unused entry in the table shall be coded FFh to indicate the end of the list of supported Applications.
Second	7-0	Module Media Interface Code	Code from Appendix C Table 79 - Table 83. The table to use is identified by the Module Type Encoding in Table 17
Third	7-4	Host Lane Count	Number of host electrical lanes 0000b=lane count defned by Application code (see Table 78) 0001b=1 lane, 0010b=2 lanes...1000b=8 lanes 1001b-1111b=reserved
	3-0	Media Lane Count	Number of module media lanes. For cable assemblies, this is the number of lanes in the cable. 0000b=lane count defined by Application code (see Table 79 - Table 83) 0001b=1 lane, 0010b=2 lanes...1000b=8 lanes 1001b-1111b=reserved

Fourth	7-0	Host Lane Assignment Options	Bits 0-7 form a bit map and correspond to Host Lanes 1-8. A bit is coded 1 if the Application is allowed to begin on the corresponding host lane. In multi-lane Applications each Application shall use contiguous host lane numbers. If multiple instances of a single Application are allowed each starting point is identified. If multiple instances are advertised, all instance must be supported concurrently.
Fifth	7-0	Media Lane Assignment Options	Bits 0-7 form a bit map and correspond to Media Lanes 1-8. A bit is coded 1 if the Application is allowed to begin on the corresponding media lane. In multi-lane Applications each Application shall use contiguous media lane numbers. If multiple instances of a single Application are allowed each supported starting point is identified. If multiple instances are advertised, all instance must be supported concurrently. This field is not required for copper cable assemblies

This specification provides space for advertisement of up to fifteen unique Applications. All modules advertise one or more Applications. The module shall advertise the Application used as the power up default in ApSel code 1. The Module Media Interface Code associated with ApSel 1 identifies the common name for the module. The module shall advertise its alternate Applications sequentially starting from ApSel code 2. Apsel codes 1-8 are advertised using Table 26, and ApSel codes 9-15 are advertised using Table 48.
Notes:

1. The advertised Application describes the host-media combination. It is the module’s responsibility to advertise only valid combinations. Hosts shall only select an advertised combination.
2. A module may use the same host interface code or the same media interface code in multiple Applications.
3. For cases where a module supports a host electrical interface code that is included in Table 78 but uses a media interface that is proprietary or not yet listed in the media interface advertising code tables, Table 79 through Table 83, the module can use a null code (00h=undefined) or a custom code for the media that the module supplier has established, combined with the host electrical interface code. The host electrical interface code and lanes provide the required information for the host to interoperate with modules that have unfamiliar or vendor-specific media types and future technologies.

The following examples illustrate some Application advertising scenarios:

Table 5 illustrates an example module advertisement for a 400GBASE-DR4 transceiver that supports breakout to 4x100G. With this example, the host could select either ApSel 1 or ApSel 2 in one of the Staged Control Sets. ApSel 1 (400GAUI-8 to 400GBASE-DR4) is the default application populated in the Active Set at power-on.

Table 5- 400GBASE-DR4 Application Advertising Example

Byte	Bits	ApSel Code	Name	Value	Description
85	7-0	N/A	Module Type encoding	02h	Optical Interfaces: SMF
86	7-0	0001b	Host Electrical Interface Code	11h	400GAUI-8 C2M
87	7-0		Module Media Interface Code	1Ch	400GBASE-DR4
88	7-4		Host Lane Count	8	8 host electrical lanes
	3-0		Media Lane Count	4	4 module media lanes
89	7-0		Host Lane Assignment Options	01h	Permissible first host lane number for Application: lane 1
176 Page 01h	7-0		Media Lane Assignment Options	01h	Permissible first media lane number for Application: lane 1
90	7-0	0010b	Host Electrical Interface Code	0Dh	100GAUI-2 C2M
91	7-0		Module Media Interface Code	14h	100GBASE-DR
92	7-4		Host Lane Count	2	2 host electrical lanes
	3-0		Media Lane Count	1	1 module media lane
93	7-0		Host Lane Assignment Options	55h	Permissible first host lane number for Application: lanes 1, 3, 5, and 7
177 Page 01h	7-0		Media Lane Assignment Options	0Fh	Permissible first media lane number for Application: lanes 1, 2, 3, 4
94	7-0	0011b	Host Electrical Interface Code	FFh	End of list of supported Applications
95	7-0		Module Media Interface Code	00h	
96	7-4		Host Lane Count	0	
	3-0		Media Lane Count	0	
97	7-0		Host Lane Assignment Options	00h	
178 Page 01h	7-0		Media Lane Assignment Options	00h	

Table 6 illustrates an example module advertisement for an 8x50G transceiver that supports breakout to a variety of lane widths. With this example, the host could select either ApSel 1, 2, 3, or 4 in one of the Staged Control Sets. ApSel 1 (400GAUI-8 to 400G-SR8) is the default application populated in the Active Set at power-on.

Table 6- 400G-SR8 Transceiver Application Advertising Example

Byte	Bits	ApSel Code	Name	Value	Description
85	7-0	N/A	Module Type encoding	01h	Optical Interfaces: MMF
86	7-0	0001b	Host Electrical Interface Code	11h	400GAUI-8 C2M
87	7-0		Module Media Interface Code	10h	400G-SR8
88	7-4		Host Lane Count	8	8 host electrical lanes
	3-0		Media Lane Count	8	8 module media lanes
89	7-0		Host Lane Assignment Options	01h	Permissible first host lane number for Application: lane 1
176 Page 01h	7-0		Media LaneAssignment Options	01h	Permissible first media lane number for Application: lane 1
90	7-0	0010b	Host Electrical Interface Code	0Fh	200GAUI-4 C2M
91	7-0		Module Media Interface Code	0Eh	200GBASE-SR4
92	7-4		Host Lane Count	4	4 host electrical lanes
	3-0		Media Lane Count	4	4 module media lanes
93	7-0		Host Lane Assignment Options	11h	Permissible first host lane number for Application: lanes 1 and 5
177 Page 01h	7-0		Media Lane Assignment Options	11h	Permissible first media lane number for Application: lanes 1, 5
94	7-0	0011b	Host Electrical Interface Code	0Dh	100GAUI-2 C2M
95	7-0		Module Media Interface Code	0Ch	100GBASE-SR2
96	7-4		Host Lane Count	2	2 host electrical lanes
	3-0		Media Lane Count	2	2 module media lanes
97	7-0		Host Lane Assignment Options	55h	Permissible first host lane number for Application: lanes 1, 3, 5, and 7
178 Page 01h	7-0		Media Lane Assignment Options	55h	Permissible first media lane number for Application: lanes 1, 3, 5, 7
98	7-0	0100b	Host Electrical Interface Code	0Ah	50GAUI-1 C2M
99	7-0		Module Media Interface Code	07h	50GBASE-SR
100	7-4		Host Lane Count	1	1 host electrical lane
	3-0		Media Lane Count	1	1 module media lane
101	7-0		Host Lane Assignment Options	FFh	Permissible first host lane number for Application: lanes 1, 2, 3, 4, 5, 6, 7, 8
179 Page 01h	7-0		Media Lane Assignment Options	FFh	Permissible first media lane number for Application: lanes 1, 2, 3, 4, 5, 6, 7, 8
102	7-0	0101b	Host Electrical Interface Code	FFh	End of list of supported Applications
103	7-0		Module Media Interface Code	00h	
104	7-4		Host Lane Count	0	
	3-0		Media Lane Count	0	

105	7-0		Host Lane Assignment Options	00h	
180 Page 01h	7-0		Media Lane Assignment Options	00h	

Table 7 illustrates an example module advertisement for an 8x50G AOC that supports one 8x50G host electrical interface or two 4x50G host electrical interfaces. With this example, the host could select either ApSel 1 or ApSel 2 in one of the Staged Control Sets. ApSel 1 (400GAUI-8) is the default application populated in the Active Set at power-on.

Table 7- 8x50G AOC Application Advertising Example

Byte	Bits	ApSel Code	Name	Value	Description
85	7-0	N/A	Module Type encoding	04h	Active cables
86	7-0	0001b	Host Electrical Interface Code	11h	400GAUI-8 C2M
87	7-0		Module Media Interface Code	03h	AOC with BER < 2.4e-4
88	7-4		Host Lane Count	8	8 host electrical lanes
	3-0		Media Lane Count	8	8 module media lanes
89	7-0		Host Lane Assignment Options	01h	Permissible first host lane number for Application: lane 1
176 Page 01h	7-0		Media Lane Assignment Options	01h	Permissible first media lane number for Application: lane 1
90	7-0	0010b	Host Electrical Interface Code	0Fh	200GAUI-4 C2M
91	7-0		Module Media Interface Code	03h	AOC with BER < 2.4e-4
92	7-4		Host Lane Count	4	4 host electrical lanes
	3-0		Media Lane Count	4	4 module media lanes
93	7-0		Host Lane Assignment Options	11h	Permissible first host lane number for Application: lanes 1 and 5
177 Page 01h	7-0		Media Lane Assignment Options	11h	Permissible first media lane number for Application: lanes 1, 5
94	7-0	0011b	Host Electrical Interface Code	FFh	End of list of supported Applications
95	7-0		Module Media Interface Code	00h	
96	7-4		Host Lane Count	0	
	3-0		Media Lane Count	0	
97	7-0		Host Lane Assignment Options	00h	
178 Page 01h	7-0		Media Lane Assignment Options	00h	

1.5.3 Data Path State Machine

A data path is defined as a combination of one or more host electrical lanes and one or more media lanes that are collectively identified by a single selected Application. A data path is created when the host selects an Application and the host lanes used for the Application through the appropriate Control Set registers. Refer to Section 1.5.2 for an overview of Applications and Section 1.5.4 for Control Set background.

Although per-lane control is provided for specific properties and controls within a data path, all lanes in a data path are powered up, initialized, and powered down as a group. The host-module interaction during this initialization process is described using a state machine. The state machine provides a state for the host to configure the data path properties (DataPathDeactivated), a state for the module to power up and initialize the hardware according to those properties (DataPathInit), a state for mission mode operation (DataPathActivated), and a state for the module to power down the data path (DataPathDeinit). Each selected Application shall have a unique and independent Data Path State Machine. If the host changes the Data Path State of one data path, the other data paths in the module shall be unaffected and uninterrupted. Module implementers should note that independent operation of data paths may require independent clocking per data path, from a recovered clock within that data path. See the Hardware specification for further information.

Figure 9 shows the Data Path State Machine for one data path instance. This common management interface specification is designed to be applied to multiple form factors. Therefore, actions and properties are described using generic terms instead of using application-specific signal names. Refer to Appendix A – Form Factor Signal Names for the association between generic descriptors in this section and application-specific signal names.

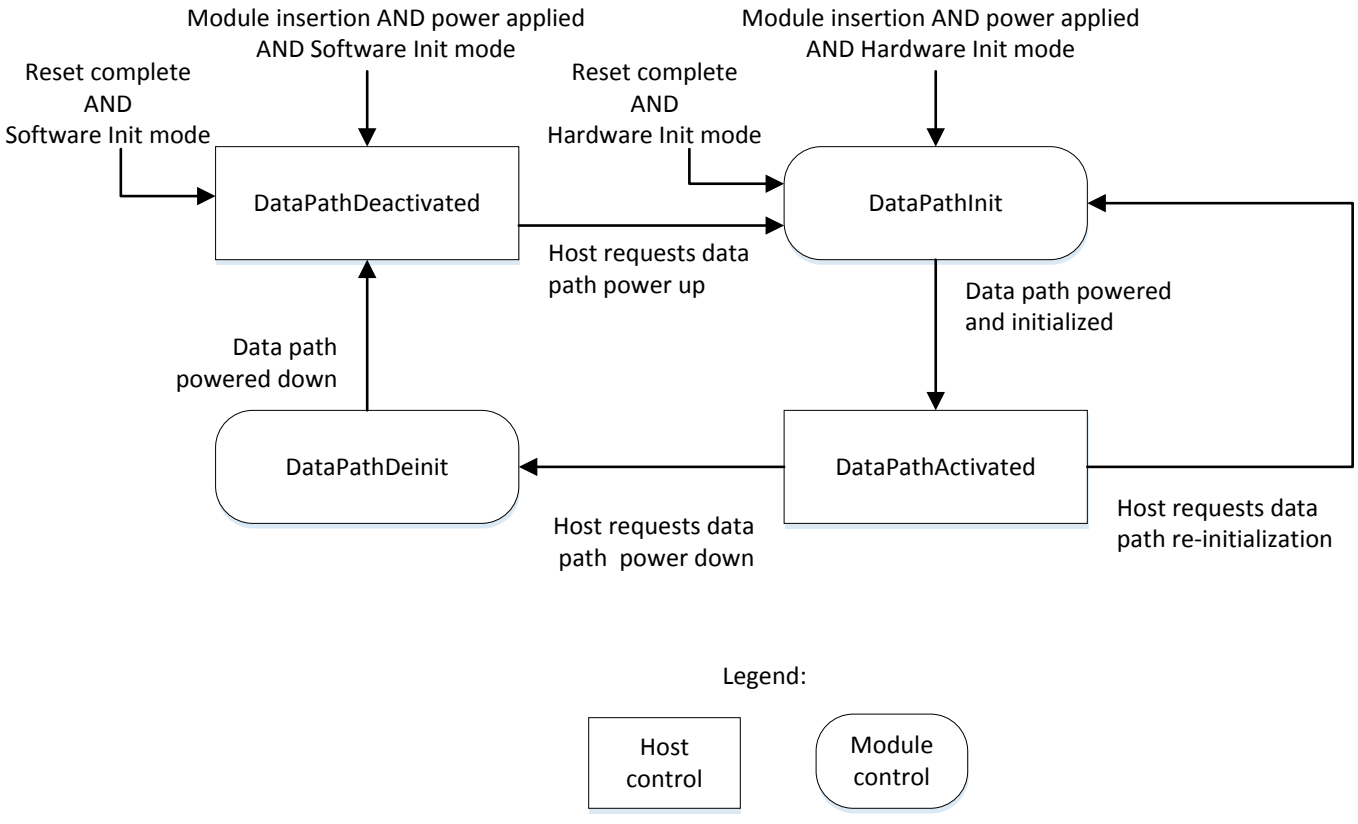

Figure 9: Data Path State Machine

The Data Path State Machine describes data path-specific behaviors and properties. For module-wide behaviors and properties, refer to the Module State Machine in Section 1.4.

States with a rectangular outline are host control states, where the module is waiting for host-initiated actions, either through the memory map or through a hardware signal. The duration of host control states is unbounded.

States with an oval outline are transient states where the module is in control of initialization activities. These module control states have an implementation-dependent duration. The maximum duration of DataPathInit and DataPathDeinit are advertised in Table 40. If either of these registers is programmed with a value of 0, that state will not be reported by the module and no interrupt will be generated when it is complete. Host interactions with the module should be avoided during all module control states. Dynamic register content is unreliable during module control states.

Table 8 provides a summary of the high-level behaviors and properties of each Data Path State for active modules. Passive copper cable assemblies do not implement paged memory and therefore do not report a Data Path State. For all module types, refer to sections 1.5.3.1-1.5.3.4 for detailed requirements for each state.

Table 8- Data path state behaviors for active modules

State	**TX output state**	**RX output state**	**Exit condition**	**Next State**
DataPathDeactivated	Quiescent	Quiescent	Host sets DataPathPwrUp bit(s)	DataPathInit
DataPathInit	Quiescent	Quiescent	Module completes data path power up and initialization	DataPathActivated
			Reset signal asserted	DataPathDeactivated
DataPathActivated	Depends on TX Disable and TX Force Squelch Table 54)	Depends on RX Output Disable Table 54)	Host clears DataPathPwrUp bit(s) OR sets ForceLowPwr bit OR asserts LowPwr signal	DataPathDeinit
			Host requests data path reconfiguration	DataPathInit
			Reset signal asserted	DataPathDeactivated
DataPathDeinit	Quiescent	Quiescent	Data path decommissioning complete OR Reset signal asserted	DataPathDeactivated

A data path is only in one state at a time. Where multiple data paths are configured, each may be in a state different from the others. The Data Path state register (Table 65) defines the current Data Path State for each lane in the module.

Certain Data Path State Machine state transitions shall cause the Data Path State Changed flag to be set, while other transitions shall not set this flag. In general, module-initiated state transitions result in the Data Path State Changed flag being set. Table 9 below defines the appropriate flag behavior for each valid state transition.

Table 9- Data Path State Change flag behaviors for active modules

Prior state	Next state	Causes Data Path State Changed flag to be set?
DataPathDeactivated	DataPathInit	No
DataPathInit	DataPathActivated	Yes
DataPathInit	DataPathDeactivated	Yes
DataPathActivated	DataPathDeinit	No
DataPathActivated	DataPathInit	No
DataPathActivated	DataPathDeactivated	Yes
DataPathDeinit	DataPathDeactivated	Yes

1.5.3.1 DataPathDeactivated State

The DataPathDeactivated state indicates that no data path is active on the indicated lane(s). The host may choose to reconfigure the number of lanes in a data path by first transitioning all candidate lanes to DataPathDeactivated, then applying the new Application Code to the applicable lanes, and finally setting the DataPathPwrUp bits to implement the new data path configuration.

The DataPathDeactivated state is a host control state that is entered when any of the following conditions occur

1) The Reset signal is asserted in Software Init mode.
2) The module is inserted and power is applied, if the module is booting in Software Init mode.
3) Any data path completes the DataPathDeinit state

Upon entry into the DataPathDeactivated state, the module shall set the Data Path state register (Table 65) for all lanes in the applicable data paths to DataPathDeactivated. If DataPathDeactivated was entered from DataPathDeinit and the DataPathDeinit_MaxDuration register is non-zero, the module shall set the Data Path State Changed flag (Table 68). The module shall not clear any interrupt flags on the state change. Interrupt flags are only cleared when the host reads the flag.

Passive modules cannot be in the DataPathDeactivated State.

All transmit and receive lane outputs associated with the data path in DataPathDeactivated shall be quiescent throughout the state. Changes to TX or RX disable or squelch for lanes in DataPathDeactivated shall have no impact on the output quiescence of those lanes.

Interrupt flag conformance in the DataPathDeactivated state is defined in Section 1.6.2. All disallowed interrupt flags shall not be set during DataPathDeactivated.

The Data Path State Machine shall only transition to DataPathInit when the host sets all of the DataPathPwrUp bits for lanes in that data path (Table 53). The Host shall provide a valid data input signal prior to setting the DataPathPwrUp bits. This input signal shall not be modified for the duration of DataPathInit. The host may power up multiple data paths in parallel by setting the DataPathPwrUp bits corresponding to multiple data paths in one write operation. Note: all of the DataPathPathPwrUp bits for each lane in a given data path must be set in a single TWI transaction. Prior to setting the DataPathPwrUp bit for all lanes in one or more data paths, the host shall provide a valid input signal at the required signaling rate and encoding type.

1.5.3.2 DataPathInit State

The DataPathInit state is a module control state that indicates that the module is performing initialization activities on the applicable data path(s). This state may be

entered due to a host-initiated action in the DataPathDeactivated or DataPathActivated states, or upon module insertion, power-up, or exit from Reset, if the module is booting in Hardware Init Mode. Initialization activities include power up of both TX and RX data path electronics, application of the selected application properties and the application and/or adaptation of signal integrity settings. The host shall provide a valid input signal at the required signaling rate and encoding type prior to entering the DataPathInit state.

Passive modules cannot be in the DataPathInit State.

Upon entry into the DataPathInit state, the module shall set the Data Path state register (Table 65) for all lanes for the applicable data paths to DataPathInit. If the module is not in High Power Mode when DataPathInit is entered, the module state machine shall be advanced to ModulePwrUp.

Within the DataPathInit state, the module shall perform power-up of all module electronics associated with the data path(s) in DataPathInit. In some cases, these electronics may be shared between multiple data paths. Depending on prior power up and down actions, some or all of the data path electronics may already be powered; in such cases, the power up sequence is bypassed. The details of the power up sequence are implementation-dependent and outside the scope of this specification.

During DataPathInit, the module shall also apply the selected application properties in the Active Set (see section 1.5.4) to the applicable module TX and RX data paths. The details of how the module applies application settings is implementation-dependent and outside the scope of this specification.

Additionally, during DataPathInit, the module shall apply the signal integrity settings in the Active Set. Entry into DataPathInit shall trigger a full initialization of the data path. For example, attributes that require adaptation, such as CTLE settings, shall be adapted at the appropriate time during DataPathInit. The order in which signal integrity settings are applied and adapted is implementation-dependent and outside the scope of this specification. Implementers should note that no input signal may be present at the input to the RX data path in the module. In such cases, the module electronics shall be fully configured, such that any adaptation or CDR locking required occurs automatically at a later point in time when an input signal is provided, without host intervention.

For all data paths in DataPathInit, all TX and RX data path outputs shall be quiescent throughout the state.

The host shall minimize TWI transactions while in this state. Dynamic memory map content may be unreliable while in this state and should not be read or written.

Interrupt flag conformance in the DataPathInit state is defined in Section 1.6.2. All disallowed interrupt flags shall not be set during DataPathInit. However, the module shall not clear any interrupt flags when exiting the DataPathInit state. Interrupt flags are only cleared when the host reads the flag.

The maximum duration of the DataPathInit state, DataPathInit_MaxDuration, includes the time to perform all of the above activities on all lanes in any data path or combination of multiple data paths for any supported Application. The DataPathInit_MaxDuration value is defined in Table 40 of the memory map. Implementers should note that this maximum duration represents the worst-case elapsed time for the module to complete the DataPathInit state. If the DataPathInit_MaxDuration register is set to 0, the worst-case duration of DataPathInit is less than 1 ms and the module will not report the state in the Data Path State register, nor report the completion of the state via the Data Path State Changed flag or Interrupt signal.

When the module has completed power-up and initialization of the applicable TX and RX data path(s), and all TX and RX data path flags, alarms, and warnings are valid, the last operation is to enable the Tx output before transitioning to DataPathActivated. Host implementers may use the Tx Disable or Tx Force Squelch bits (Table 54) to prevent the module from enabling the Tx output at the end of DataPathInit. Once the Tx output is enabled and stabilized or the module identifies that the host has set Tx Disable or Tx Force Squelch the data path shall transition to the DataPathActivated state.

1.5.3.3 DataPathActivated State

The DataPathActivated state is a host control state. Data paths that are in the DataPathActivated state are considered fully initialized and ready to transmit live traffic.

Upon entry into the DataPathActivated state, the module shall set the Data Path state register (Table 65) for all lanes in the applicable data paths to the DataPathActivated state. If the DataPathInit_MaxDuration register is non-zero or the module is completing a Hardware Init mode boot, the module shall set the Data Path State Changed flag (Table 68). The module shall not clear any interrupt flags on the state change. Interrupt flags are only cleared when the host reads the flag.

Interrupt flag conformance in the DataPathActivated state is defined in Section 1.6.2. All disallowed interrupt flags shall not be set during DataPathActivated.

For active modules, the module shall be in High Power Mode when any data path is in the DataPathActivated State.

The host may enable, disable or squelch TX or RX outputs at any time for any lane whose data path is in the DataPathActivated State. If the host has set TX or RX disable or squelch prior to entry into DataPathActivated, the applicable lane outputs shall remain disabled or squelched throughout the transition from DataPathInit into DataPathActivated. Host implementers should note that for certain optical implementations a change to the Tx disable bits may require additional time for laser stabilization.

For active modules, the data path shall transition to the DataPathDeinit state if the host clears the applicable bit in the DataPathPwrUp register, including modules that booted in Hardware Init mode. The host may transition multiple data paths to DataPathDeinit simultaneously by clearing multiple DataPathPwrUp bits in a single write transaction or by setting the ForceLowPwr bit or asserting the LowPwr signal.

The host may alternatively choose to reconfigure one or more data paths while in DataPathActivated by applying a new Application in one of the Staged Control Sets to the applicable data paths using Apply_DataPathInit. To cause a transition to DataPathInit, the host shall set all Apply_DataPathInit bits associated with that data path. Multiple data paths may be reinitialized at the same time. Prior to setting the DataPathPwrUp bit for all lanes in one or more data paths, the host shall provide a valid input signal at the required signaling rate and encoding type. Module implementers should note that data paths excluded from the Apply_DataPathInit lane mask shall not transition Data Path States nor change data path properties. This selective control allows host reconfiguration of individual data paths in breakout Applications without affecting the operation of other data paths in the module.

1.5.3.4 DataPathDeinit State

The DataPathDeinit state is a module control state that is entered only through one of three host-initiated actions

1) The host clears the DataPathPwrUp bit for all lanes in the applicable data path (Table 53).
2) The host sets the ForceLowPwr bit (Table 23).
3) The host asserts the LowPwr signal.

Upon entry into the DataPathDeinit state, the module shall set the Data Path state register (Table 65) for the applicable lanes to the DataPathDeinit state and disable the Tx output.

During DataPathDeinit, the module may power down applicable data path electronics. In some cases, electronics may be shared with other data paths that are still in the DataPathInit or DataPathActivated states. In such cases, these electronics shall remain powered. Similarly, module implementers may identify certain electronics that require significant power up times. Module implementers may choose to keep these electronics powered even when the host requests data path power down. If the host wants to ensure maximum power savings, the host may initiate a module transition to Low Power Mode by setting the ForceLowPwr bit or asserting the LowPwr signal. Throughout DataPathDeinit, the module may be in High Power Mode.

For all data paths in DataPathDeinit, all TX and RX data path outputs shall be quiescent throughout the state. Changes to TX or RX disable or squelch for lanes in DataPathDeinit shall have no impact on the output quiescence of those lanes.

The host shall minimize TWI transactions while in this state. Dynamic memory map content may be unreliable for lanes in this state and should not be read or written.

Interrupt flag conformance in the DataPathDeinit state is defined in Section 1.6.2. All disallowed interrupt flags shall not be set during DataPathDeinit. However, the module shall not clear any interrupt flags on the state change. Interrupt flags are only cleared when the host reads the flag or sends a reset signal.
The maximum duration of the DataPathDeinit state, DataPathDeinit_MaxDuration, includes the time to perform all of the above activities on all lanes in any data path or combination of multiple data paths for any supported Application. The DataPathDeinit_MaxDuration value is defined in Table 40. Implementers should note that this maximum duration represents the worst-case elapsed time for the module to complete the DataPathDeinit state. If the DataPathDeinit_MaxDuration register is set to 0, the worst-case duration of DataPathDeinit is less than 1 ms and the module will not report the state in the DataPathState register, nor report the completion of the state via the Data Path State Changed flag or Interrupt signal.

When the module has completed applicable power down activities, the data path shall be disbanded and all lanes shall transition to the DataPathDeactivated state.

1.5.4 Control Set Overview

A Control Set is a group of registers that are used to provide initialization settings for data paths. Each control set includes fields to select the Application, fields for signal integrity control, and fields to apply these Application and signal integrity settings.

Within a Control Set, the host uses the Application Select Control registers defined in Table 56 or Table 60 to select the desired Application(s) and configure the data path(s) within the module. The Application Select Control registers include an ApSel code, a Data Path Code and an Explicit Control bit.

Each supported Application advertised in Table 26 and Table 48 is identified by an ApSel code. The host uses the ApSel code to assign that Application to one or more specific lanes using the Application Select Control registers. Where an Application requires multiple lanes, the host shall write the same ApSel code into each lane of that Application.

The Data Path Code in the Application Select Control registers is used to specify the lanes used for an instance of an Application. Each data path is identified by the lowest numbered lane in that data path. The host shall assign lane combinations that are in

accordance with the lane assignment advertised by the module for that application. For a multi-lane data path the host shall write the same data path code in all lanes of that data path.

The Explicit Control bit allows the host to provide either its own signal integrity values or use the Application-defined signal integrity values associated with the ApSel code. These Application-defined settings shall provide host electrical and media interfaces that are compliant with the standard associated with the selected Application. To use Explicit Control for a given lane (by setting the control bit to '1'), the host shall provide values for all signal integrity controls for that lane in the Control Set.

The value of the Explcit Control bit determines which signal integrity control fields within the Control Set are used in an Apply operation. When the Explicit Control bit for a given lane is set to the value listed in Table 10, the associated control field value for that lane is used in an Apply operation. The control field value for that lane is ignored for all other values of the Explicit Control bit.

Table 10- Control field dependency on Explicit Control bit

Control field	Explicit Control value
Tx Adaptive Input Eq Enable	1
Tx Adaptive Input Eq Recall	1 or 0
Tx Input Eq control	1
Tx CDR control	1
Rx CDR control	1
Rx Output Eq control, pre-cursor	1
Rx Output Eq control, post-cursor	1
Rx Output Amplitude control	1

The usage of these signal integrity control fields is defined in Section 1.5.5.

1.5.4.1 Control Set Usage

There are two types of control sets. The Active Control Set reports the current settings that are used by the module to control its hardware. The Staged Control Sets are used by the host to identify new settings for future use. Apply-fields are used to copy those settings from the Staged Control Set registers into the Active Control Set registers. This apply mechanism decouples the timing and sequence of host writes to the Staged Control Set from the module actions used to configure the module hardware. Each module shall implement the Active Control Set and at least one host-configurable Staged Control Set.

When the host requests power up of a data path, the module shall use the settings in the Active Control Set for data path initialization. Those settings may have been copied from the Staged Control Set by a previous host Apply action, or those settings may have been programmed into the Active Set as power-on defaults. The module shall populate both Staged Control Set 0 and the Active Control Set registers with the module-defined default Application and signal integrity settings at power on or exit from reset.

There are two controls that can be used to copy the settings from a Staged Control Set to the Active Control Set on a per lane basis: Apply_DataPathInit and Apply_Immediate. When used in the DataPathDeactivated State the Apply_DataPathInit and Apply_Immediate controls only copy the settings into the Active Control Set and do not cause a transition in the Data Path State Machine (see Section 1.5.3 for Data Path State Machine details). When the host requests data path power up, the Data Path State Machine shall transition to DataPathInit, regardless of which Apply mechanism was used.

When used in the DataPathActivated State, the Apply_DataPathInit control copies the Staged Control Set into the Active Control Set and performs a full re-initialization of the data path. In this scenario, the Apply action must be performed on all lanes in the data path at the same time. Use of Apply_DataPathInit in the DataPathActivated state may be disruptive because the Data Path State Machine returns to DataPathInit, where the transmitters are disabled. In cases where new settings need to be applied quickly without disabling the transmitters, such as Fibre Channel Link Speed Negotiation (LSN), the host should use the Apply_Immediate control. This control does not transition the Data Path State Machine out of DataPathActivated. Host implementers should note that the host is required to transition the data path state to DataPathDeactivated before the host selects an Application with a different lane count.

The module may report the acceptance or rejection of the requested configuration using the Configuration Error Code registers in Table 71. If accepted, the module shall copy the configuration into the Active Set and change the data path state. If the configuration is rejected, the module shall abort the Apply operation without copying the settings. The Configuration Error Code shall be reported on all applicable lanes and may differ from data path to data path.

Figure 10 illustrates the flow of Control Set settings from the Staged Set into the Active set and module hardware.

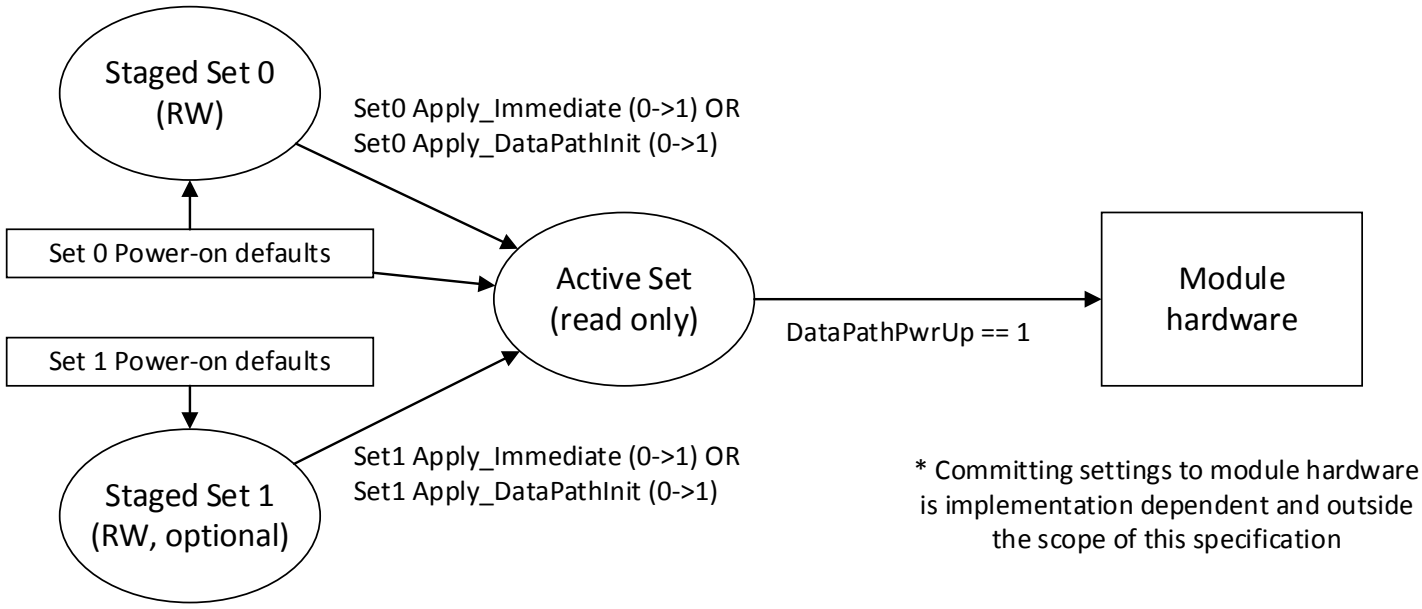

Figure 10: Control Set Data Flow Diagram

The translation of memory map settings to the module hardware is implementation-specific and outside the scope of this specification. Module implementers should use a best effort approach when trying to translate memory map settings to module hardware settings.

If the host sets the same bits in both Apply_DataPathInit and Apply_Immediate in the same two-wire serial transaction, the Apply_DataPathInit bit shall take precedence. The host shall not set bits for Apply_DataPathInit or Apply_Immediate when the corresponding data path is in DataPathInit or DataPathDeinit; the module may ignore such requests.

1.5.4.2 Initialization Sequence Examples

The data path architecture described above is intentionally designed to support a broad array of implementations while ensuring compatibility across hosts and modules. Some Applications may not use all of the features provided in the architecture. Appendix B – Host-Module Initialization Example Flows, contains some example host-module initialization flows that can be used for popular Applications.

1.5.5 Signal Integrity Control Field Background

The signal integrity control fields provide an opportunity for the host to specify signal integrity settings to the module. For each control, the host sets the code for the desired behavior and the device makes a best effort to provide the function indicated.

The Tx Input Equalizer has multiple controls associated with it. These controls can be divided into two groups: those that are active when Tx Adaptive Input Eq is enabled and those that are active when Tx Adaptive Input Eq is disabled. Table 11 summarizes which controls are associated with each group. The module shall ignore the value in the applicable control field when the Tx Adaptive Input Eq Enable bit is not set to use that control (see Table 11).

Table 11- Tx Input Eq control relationship to Tx Adaptive Input Eq Enable

Control	Tx Adaptive Input Eq Enable value to use this control
Tx Input Eq Adaptation Freeze	1
Tx Input Eq Adaptation Store	1
Tx Adaptive Input Eq Recall	1
Tx Input Eq control	0

The Tx Input Equalization Control is a four-bit field per lane as shown in Table 12. This field allows the host to specify fixed Tx input equalization and is ignored by the module if Tx Adaptive Input Eq Enable is set for that lane. Refer to Table 46 to determine if the module supports Fixed Tx Input Equalization Control. Refer to Table 42 for the Maximum Tx equalization supported by the module. The code values and the corresponding input equalization are based on a reference CTLE and may not directly apply to the equalizer implemented in the module.

Table 12- Fixed Tx Input Equalization Codes

Code Value	Bit pattern	Input Equalization
0	0000	No Equalization
1	0001	1 dB
2	0010	2 dB
3	0011	3 dB
4	0100	4 dB
5	0101	5 dB
6	0110	6 dB
7	0111	7 dB
8	1000	8 dB
9	1001	9 dB
10	1010	10 dB
11	1011	11 dB
12	1100	12 dB
13-15		Custom

The Rx Output Emphasis Control is a four-bit field per lane. Refer to Table 46 to determine if the module supports Rx Output Emphasis Control. Refer to Table 42 for the maximum Rx output emphasis supported by the module. Rx output emphasis is defined at the

appropriate test point defined by the relevant standard. The code values and the corresponding output equalization are defined as follows:

Table 13- Rx Output Emphasis Codes

Code Value	Bit pattern	Post-Cursor Equalization	Pre-Cursor Equalization
0	0000	No Equalization	No Equalization
1	0001	1 dB	0.5 dB
2	0010	2 dB	1.0 dB
3	0011	3 dB	1.5 dB
4	0100	4 dB	2.0 dB
5	0101	5 dB	2.5 dB
6	0110	6 dB	3.0 dB
7	0111	7 dB	3.5 dB
8-10	1000-1010	Reserved	Reserved
11-15	1011-1111	Custom	Custom

Note: The pre-cursor equalizer settings in dB approximates to
Pre EQ (dB)=-20*log10((1-(C(-1)/(C(-1)+C(0)+C(1))
The post-cursor equalizer settings in dB approximates to
Post EQ (dB)=-20*log10(1-(C(1)/(C(-1)+C(0)+C(1))

The Rx Output Amplitude Control is a four-bit field per lane. The output amplitude is measured with no equalization enabled. Refer to Table 46 to determine if the module supports Rx Output Amplitude Control and Table 42 to determine which codes are supported. Output amplitude is defined at the appropriate test point defined by the relevant standard. The code values and the corresponding output amplitude are defined as follows:

Table 14- Rx Output Amplitude Codes

Code Value	Bit pattern	Output Amplitude
0	0000	100-400 mV (P-P)
1	0001	300-600 mV (P-P)
2	0010	400-800 mV (P-P)
3	0011	600-1200 mV (P-P)
4-14	0100-1110	Reserved
15	1111	Custom

1.5.5.1 Tx Input Eq Adaptation Store/Recall Methodology

Transmit equalizer adaptation can be a time-consuming activity. In some implementations, the available time for a speed change does not include equalizer adaptation time. This specification provides an optional Tx Input Eq Adaptation Store and Recall mechanism, to facilitate storing of adapted equalizer values for recall and use at a later time.

Module support of the Tx input Eq Adaptation Store and Recall mechanism is optional and declared in Table 46. This advertisement field identifies the number of Store/Recall buffers implemented in the module. These buffers are independent of Staged Set 0 and 1 and may be numbered independently. The module shall provide sufficient storage in each Store/Recall buffer to store the adapted equalizer value for each lane in the module. This storage is implementation specific and not defined in this specification.

The Tx Input Eq Adaptation Store control field is located in
Table 54. This field provides two bits per lane and is write only. A read of this register shall return 0. When the host would like to store the most recent adapted Tx input equalizer value, the host shall write the target store location encoding into the Tx Input Eq Adaptation Control, into each lane whose adapted value should be stored. Adaptation shall continue to occur after the store event completes unless the Tx Input Eq

Adaptation Freeze bit is set. Host requests to store the Tx Input Eq Adaptation when the Tx Input Eq Adaptation Enable bit for that lane is clear shall be ignored by the module. Tx Input Eq Adaptation Store may occur at any time while a data path is powered and occurs when requested.

The Tx Input Eq Adaptation Recall control field is located in Table 57 for Staged Set 0 and Table 61 for Staged Set 1. This field provides two bits per lane and is read-write. The Active Set provides a read-only indication of the current Tx Input Eq Adaptation Recall status for each lane. The host may recall any stored Tx Input Eq Adaptation by programming the applicable lane controls with the store location to be recalled. These values are not recalled until the Apply_DataPathInit or Apply_Immediate bits are 1 for that Staged Set.

The Tx Input Eq Adaptation Recall field is used independent of the Explicit Control field settings for that lane. If the Tx input freeze bit is clear, the recalled Tx input eq adaptation shall be used as the starting point for continuous adaptation for the applicable lanes. If the Tx Input Eq Freeze bit is set, the recalled Tx Input Eq Adaptation shall be used as the frozen Tx Input Eq value for the applicable lanes.

1.6 Interrupt Flag Conformance per State

Some flags are generated by the Module or Data Path State Machines, but the majority of flags are triggered by other sources. In some states, certain flags are not applicable and should be inhibited. The following sections define the conformance for all interrupts for each state in the Module and Data Path State Machines.

1.6.1 Module Flag Conformance per State

Table 15 describes the flag conformance for all module flags, per module state. In module states where a flag is indicated as ‘Not Allowed’, the module shall not set the associated flag bit while the module is in that state. All module flags shall be ‘Not Allowed’ throughout the Reset and MgmtInit states. Module flag conformance is not dependent on Data Path State. Some module interrupts are module-configurable; Table 15 defines the flag conformance for each configuration option for those flags. Host implementers should note that if certain interrupts are undesirable, the host may mask those interrupts by setting the corresponding interrupt mask bit at any time after the management interface is initialized.

Table 15- Module Flag Conformance

Flag	Page	Byte	ModuleLowPwr Fault	ModulePwrUp ModulePwrDn ModuleReady
Module state change	00h	8	Allowed	Allowed
Module temperature	00h	9	Allowed	Allowed
Vcc 3.3V	00h	9	Allowed	Allowed
Aux1 – TEC Current	00h	10	Not Allowed	Allowed
Aux2 – TEC temp	00h	10	Not Allowed	Allowed
Aux2 – Laser temp	00h	10	Not Allowed	Allowed
Aux3 – Laser temp	00h	11	Not Allowed	Allowed
Aux3 – addl voltage	00h	11	Allowed	Allowed
Vendor-defined	00h	11	See below	Allowed

The vendor-defined flag is Allowed in ModuleLowPwr if and only if it applies to a feature that is available in Low Power Mode.

1.6.2 Lane-Specific Flag Conformance per State

Table 16 describes the flag conformance for all lane-specific flags, per Data Path State. In Data Path States where a flag is indicated as 'Not Allowed', the module shall not set the associated flag bit while the data path is in that state. All lane-specific flags shall be 'Not Allowed' throughout the Reset and MgmtInit module states. For all other module states, implementers should refer to the Data Path State to determine lane-specific flag conformance. Host implementers should note that if certain interrupts are undesirable, the host may mask those interrupts by setting the corresponding interrupt mask bit at any time after the management interface is initialized.

Table 16- Lane-Specific Flag Conformance

Flag	Page	Byte	DataPath Deactivated	DataPath Activated	DataPathInit	DataPathDeinit
Data Path State Change[1]	11h	134	Allowed	Allowed	Allowed	Allowed
TX Fault	11h	135	Allowed	Allowed	Allowed	Allowed
TX LOS	11h	136	Not Allowed	Allowed	Not Allowed	Not Allowed
TX CDR LOL	11h	137	Not Allowed	Allowed	Not Allowed	Not Allowed
TX Adaptive Input Eq Fault	11h	138	Not Allowed	Allowed	Allowed	Not Allowed
Tx output power High Alarm	11h	139	Allowed	Allowed	Allowed	Allowed
Tx output power Low alarm	11h	140	Not Allowed	Allowed	Not Allowed	Not Allowed
Tx output power High warning	11h	141	Allowed	Allowed	Allowed	Allowed
Tx output power Low warning	11h	142	Not Allowed	Allowed	Not Allowed	Not Allowed
Tx Bias High Alarm	11h	143	Allowed	Allowed	Allowed	Allowed
Tx Bias Low alarm	11h	144	Not Allowed	Allowed	Not Allowed	Not Allowed
Tx Bias High warning	11h	145	Allowed	Allowed	Allowed	Allowed
Tx Bias Low Warning	11h	146	Not Allowed	Allowed	Not Allowed	Not Allowed
RX LOS	11h	147	Allowed	Allowed	Allowed	Allowed
RX CDR LOL	11h	148	Not Allowed	Allowed	Not Allowed	Not Allowed
RX Input Pwr High Alarm	11h	149	Allowed	Allowed	Allowed	Allowed
RX Input Power Low alarm	11h	150	Not Allowed	Allowed	Not Allowed	Not Allowed
RX Input Power High warning	11h	151	Allowed	Allowed	Allowed	Allowed
RX Input Power Low warning	11h	152	Not Allowed	Allowed	Not Allowed	Not Allowed

Note 1: The Data Path State Changed flag is only allowed when the module is transitioning from DataPathInit to DataPathActivated or DataPathDeinit to DataPathDeactivated. When the module is entering DataPathInit or DataPathDeinit, the module shall not assert the Data Path State Changed Flag. If the advertised DataPathInit_MaxDuration encoding is 0 (See Table 40), then the module shall not set the Data Path State Changed Flag when transitioning from DataPathInit to DataPathActivated. If the advertised DataPathDeinit_MaxDuration encoding is 0 (see Table 40), then the module shall not set the Data Path State Changed Flag when transitioning from DataPathDeinit to DataPathDeactivated

1.7 Module Memory Map

This subsection defines the Memory Map for a CMIS Module used for serial ID, digital monitoring and certain control functions. The interface is mandatory for all CMIS devices. The interface has been designed largely after the QSFP memory map. The memory map has been changed in order to accommodate 8 electrical lanes and limit the required memory space. The single address approach is used as found in QSFP. Paging is used in order to enable time critical interactions between host and module.

The structure of the memory is shown in Figure 11. The memory space is arranged into a lower, single page, address space of 128 bytes and multiple upper address space pages. This structure supports a flat 256 byte memory for passive copper cables and permits timely access to addresses in the lower page, e.g. Flags and Monitors. Less time critical entries, e.g. serial ID information and threshold settings, are available with the Page Select function.

The structure also provides address expansion by adding additional upper pages as needed. Upper pages 00-02 all contain static, non-volatile advertising registers. Upper page 01 provides revision codes and advertising registers that indicate the capabilities of the module. Upper page 02 provides thresholds for monitored functions. Upper page 03 provides a user read/write space. The lower page and upper page 00 are required for passive copper cables and are always implemented. In addition, upper pages 1, 2 and bank 0 pages 10h and 11h are required for active modules. See Table 40 for details regarding the implementation of optional upper pages and the bank pages.

Bank pages are provided to provide the ability to support modules with more than 8 lanes. For pages 10h-1Fh, Bank 0 provides lane-specific registers for the lower 8 lanes, and each additional bank provides support for an additional 8 lanes. Note, however, the bank structure may be page specific and not be related to 8 lanes.

Reserved bytes are for future use and shall not be used and shall be set to 0. Other organizations shall contact the managing organization or the editor of this document to request allocations of registers. The use of custom bytes is not restricted and may be vendor defined. The use of registers defined as custom may be subject to additional agreements between module users and vendors.

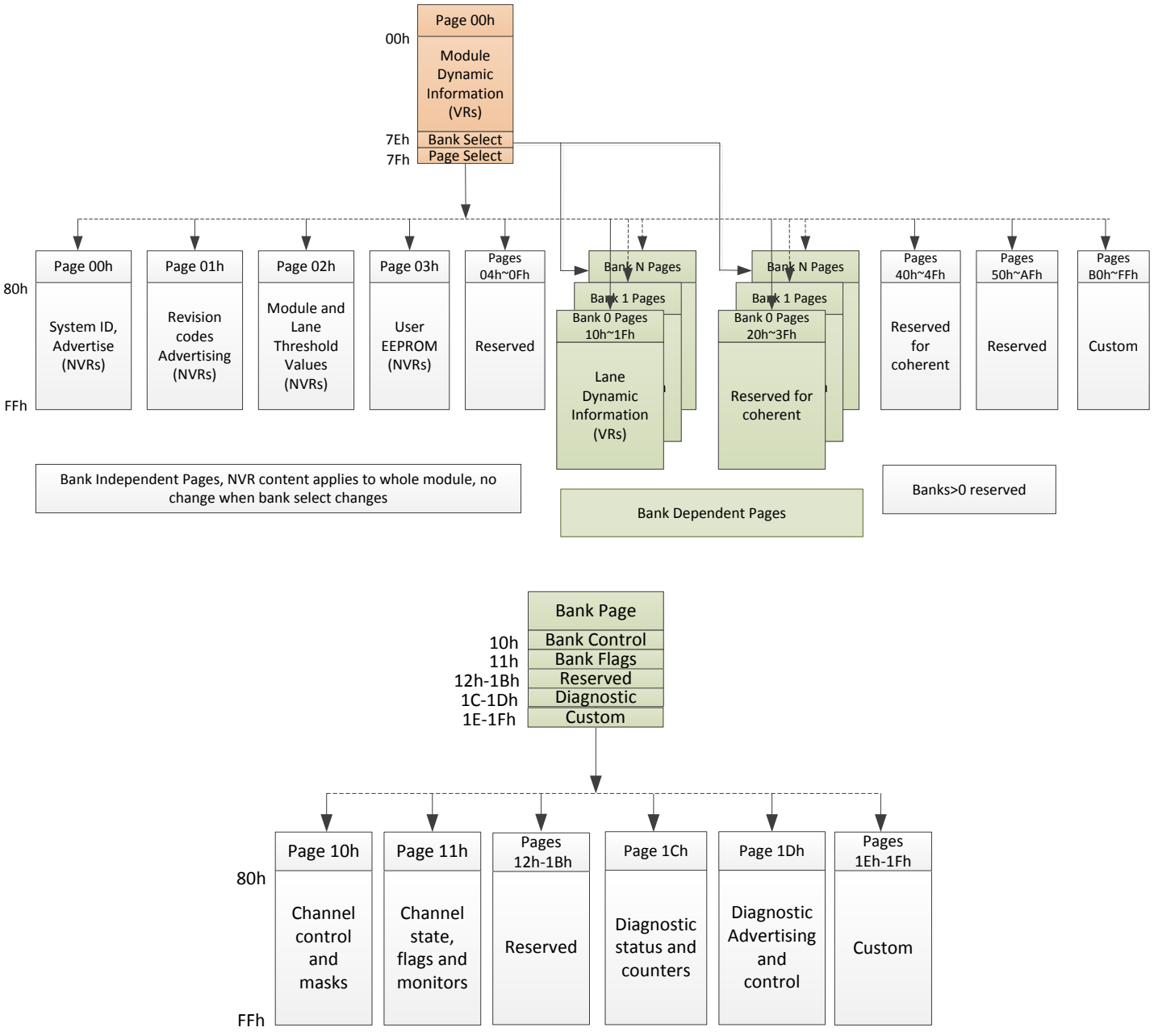

Figure 11: CMIS Module Memory Map

1.7.1 Register default values

Default values for all control registers are 0 unless otherwise specified. Host implementers are encouraged to review critical registers and not rely on module default values. For Control Set registers the default settings may be Application dependent. See Section 1.5.4.

1.7.2 Lower Page 00h

The lower 128 bytes of the two-wire serial bus address space is used to access a variety of module level measurements, diagnostic functions and control functions, as well as a means to select which of the various upper memory map pages are accessed on subsequent accesses. This portion of the address space is always directly addressable and thus is chosen for monitoring and control functions that may need to be repeatedly accessed.

The lower page is subdivided into several areas as illustrated in the following table:

Table 17- Lower Page Overview (Lower Page)

Address	Size	Name	Description
0–1	2	Id and version ID	Module ID from SFF-8024 list, version number, Type and status
2-3	2	Flat mem, CLEI present, TWI speed, Module State, Interrupt	Flat mem indication, CLEI present indicator, Maximum TWI speed, Current state of Module, Current state of the Interrupt signal
4–7	4	Bank Lane Flag Summary	Flag summary of all lane flags on pages 10h-1Fh
8-13	6	Module Flags	All flags that are module wide (i.e. not lane specific)
14-25	12	Module Monitors	
26-30	5	Module Global Controls	
31-36	6	Module masks	Module flag masks
37-63	27	Reserved	
64-84	21	Custom	
85	1	Module Type advertising code	
86-117	32	Module Host-Media Interface Advertising Options	Host and media interfaces that are supported by the module
118-125	8	Password area	
126	1	Bank Select Byte	
127	1	Page Select Byte	

1.7.2.1 ID and Status

The ID and Status fields described in Table 18 provide fundamental memory map characteristics (module type, flat or paged memory, memory map version) as well as module status indicators.

Table 18- Identifier and Status Summary (Lower Page)

Byte	Bits	Name	Description	Type
0	7-0	Identifier	Identifier - Type of Serial Module - See SFF-8024.	RO RQD
1	7-0	Revision Compliance	Identifier – CMIS revision; the upper nibble is the whole number part and the lower nibble is the decimal part. Example: 01h indicates version 0.1, 21h indicates version 2.1.	RO RQD
2	7	Flat_mem	Upper memory flat or paged. 0b=Paged memory (pages 01h, 02h, 10h and 11h are implemented) 1b=Flat memory (only page 00h implemented)	RO RQD
	6	CLEI present	CLEI code present in upper page 00h	
	5-4	Reserved		
	3-2	TWI Maximum speed	Indicates maximum two-wire serial speed supported by module 00b=Module supports up to 400 kHz 01b=Module supports up to 1 MHz 10b=Reserved 11b=Reserved	RO RQD
	1-0	Reserved		
3	7-4	Reserved		
	3-1	Module state	Current state of Module (see Table 19)	RO RQD
	0	Interrupt	Digital state of Interrupt output signal 0b=Interrupt asserted 1b=Interrupt not asserted (default)	

Table 19- Module State Encodings

Code	Module state
000b	Reserved
001b	ModuleLowPwr state(Flat memory passive cable assemblies)
010b	ModulePwrUp state
011b	ModuleReady state
100b	ModulePwrDn state
101b	Fault state
110b	Reserved
111b	Reserved

1.7.2.2 Lane Flag Summary

The lane flag summary bits identify which lane(s) flags are asserted in page 11h, for up to 4 banks of lanes. In order to clear the lane-specific flag, the lane flag itself must be read from page 11h on the appropriate bank.

Table 20- Lane Flag Summary (Lower Page)

Byte	Bit	Name	Description	Type
4	7	Bank 0 lane 8 flag summary	1b=one or more of the flag bits from bank 0, lane 8 is set.	RO RQD
	6	Bank 0 lane 7 flag summary	1b=one or more of the flag bits from bank 0, lane 7 is set.	RO RQD
	5	Bank 0 lane 6 flag summary	1b=one or more of the flag bits from bank 0, lane 6 is set.	RO RQD
	4	Bank 0 lane 5 flag summary	1b=one or more of the flag bits from bank 0, lane 5 is set.	RO RQD

	3	Bank 0 lane 4 flag summary	1b=one or more of the flag bits from bank 0, lane 4 is set.	RO RQD
	2	Bank 0 lane 3 flag summary	1b=one or more of the flag bits from bank 0, lane 3 is set.	RO RQD
	1	Bank 0 lane 2 flag summary	1b=one or more of the flag bits from bank 0, lane 2 is set.	RO RQD
	0	Bank 0 lane 1 flag summary	1b=one or more of the flag bits from bank 0, lane 1 is set.	RO RQD
5	7	Bank 1 lane 8 flag summary	1b=one or more of the flag bits from bank 1, lane 8 is set.	RO RQD
	6	Bank 1 lane 7 flag summary	1b=one or more of the flag bits from bank 1, lane 7 is set.	RO RQD
	5	Bank 1 lane 6 flag summary	1b=one or more of the flag bits from bank 1, lane 6 is set.	RO RQD
	4	Bank 1 lane 5 flag summary	1b=one or more of the flag bits from bank 1, lane 5 is set.	RO RQD
	3	Bank 1 lane 4 flag summary	1b=one or more of the flag bits from bank 1, lane 4 is set.	RO RQD
	2	Bank 1 lane 3 flag summary	1b=one or more of the flag bits from bank 1, lane 3 is set.	RO RQD
	1	Bank 1 lane 2 flag summary	1b=one or more of the flag bits from bank 1, lane 2 is set.	RO RQD
	0	Bank 1 lane 1 flag summary	1b=Indicates that one or more of the flag bits from bank 1, lane 1 is set.	RO RQD
6	7	Bank 2 lane 8 flag summary	1b=one or more of the flag bits from bank 2, lane 8 is set.	RO RQD
	6	Bank 2 lane 7 flag summary	1b=one or more of the flag bits from bank 2, lane 7 is set.	RO RQD
	5	Bank 2 lane 6 flag summary	1b=one or more of the flag bits from bank 2, lane 6 is set.	RO RQD
	4	Bank 2 lane 5 flag summary	1b=one or more of the flag bits from bank 2, lane 5 is set.	RO RQD
	3	Bank 2 lane 4 flag summary	1b=Indicates that one or more of the flag bits from bank 2, lane 4 is set.	RO RQD
	2	Bank 2 lane 3 flag summary	1b=Indicates that one or more of the flag bits from bank 2, lane 3 is set.	RO RQD
	1	Bank 2 lane 2 flag summary	1b=Indicates that one or more of the flag bits from bank 2, lane 2 is set.	RO RQD
	0	Bank 2 lane 1 flag summary	1b=Indicates that one or more of the flag bits from bank 2, lane 1 is set.	RO RQD
7	7	Bank 3 lane 8 flag summary	1b=one or more of the flag bits from bank 3, lane 8 is set.	RO RQD
	6	Bank 3 lane 7 flag summary	1b=one or more of the flag bits from bank 3, lane 7 is set.	RO RQD
	5	Bank 3 lane 6 flag summary	1b=one or more of the flag bits from bank 3, lane 6 is set.	RO RQD
	4	Bank 3 lane 5 flag summary	1b=one or more of the flag bits from bank 3, lane 5 is set.	RO RQD
	3	Bank 3 lane 4 flag summary	1b=one or more of the flag bits from bank 3, lane 4 is set.	RO RQD
	2	Bank 3 lane 3 flag summary	1b=one or more of the flag bits from bank 3, lane 3 is set.	RO RQD
	1	Bank 3 lane 2 flag summary	1b=one or more of the flag bits from bank 3, lane 2 is set.	RO RQD
	0	Bank 3 lane 1 flag summary	1b=one or more of the flag bits from bank 3, lane 1 is set.	RO RQD

1.7.2.3 Module-Level Flags

This section of the memory map contains module-level flags. These flags provide a mechanism for reporting module-level alarms and warnings for monitored module conditions. If a module-level monitor is implemented with the associated alarm and warning thresholds, the alarm and warning flags and flag masks must also be implemented. For normal operation and default state, the bits in this field have the value of 0b. Once asserted, the bits remain set (latched) until cleared by a read operation that includes the affected bit or reset by the Reset signal. Note that a read of the flag summary shall not clear the underlying flag condition. If the corresponding mask bit is not set (see Table 24), Interrupt is also asserted at the onset of the condition and remains asserted until all asserted flags (both module-level and lane-specific) have been cleared by a host read. After being read and cleared, the bit shall be set again if the condition persists; this will cause Interrupt to be asserted again unless masked. The Module level Flags are defined in Table 21. Byte 12 is reserved for future Module level flags. Byte 13 is provided for Custom Module Level Flags. Some module-level flags are disallowed in certain Module States, refer to section 1.6.1 for details.

Table 21- Module Flags (Lower Page, active modules only)

Byte	Bit	Name	Description	Type
8	7-3	Reserved		RQD
	2	Data Path firmware fault	Some modules may contain an auxiliary device for processing the transmitted and received signals (e.g. a DSP). The Datapath Firmware Fault flag becomes set when an integrity check of the firmware for this auxiliary device finds an error.	RO Opt.
	1	Module firmware fault	The Module Firmware Fault flag becomes set when an integrity check of the module firmware finds an error. There are several possible causes of the error such as program memory becoming corrupted and incomplete firmware loading.	RO Opt.
	0	L-Module state changed flag	Latched Indication of change of Module state (see Table 3)	RO RQD
9	7	L-Vcc3.3v Low Warning	Latched low 3.3 volts supply voltage warning flag	RO Opt.
	6	L-Vcc3.3v High Warning	Latched high 3.3 volts supply voltage warning flag	
	5	L-Vcc3.3v Low Alarm	Latched low 3.3 volts supply voltage alarm flag	
	4	L-Vcc3.3v High Alarm	Latched high 3.3 volts supply voltage alarm flag	
	3	L-Temp Low Warning	Latched low temperature warning flag	
	2	L-Temp High Warning	Latched high temperature warning flag	
	1	L-Temp Low Alarm	Latched low temperature alarm flag	
	0	L-Temp High Alarm	Latched high temperature alarm flag	
10	7	L-Aux 2 Low Warning	Latched low warning for Aux 2 monitor	RO Opt.
	6	L-Aux 2 High Warning	Latched high warning for Aux 2 monitor	
	5	L-Aux 2 Low Alarm	Latched low alarm for Aux 2 monitor	
	4	L-Aux 2 High Alarm	Latched high alarm for Aux 2 monitor	
	3	L-Aux 1 Low Warning	Latched low warning for Aux 1 monitor	
	2	L-Aux 1 High Warning	Latched high warning for Aux 1 monitor	
	1	L-Aux 1 Low Alarm	Latched low alarm for Aux 1 monitor	
	0	L-Aux 1 High Alarm	Latched high alarm for Aux 1 monitor	

11	7	L-Vendor Defined Low Warning	Latched low warning for Vendor Defined Monitor	RO Opt.
	6	L-Vendor Defined High Warning	Latched high warning for Vendor Defined Monitor	
	5	L-Vendor Defined Low Alarm	Latched low alarm for Vendor Defined Monitor	
	4	L-Vendor Defined High Alarm	Latched high alarm for Vendor Defined Monitor	
	3	L-Aux 3 Low Warning	Latched low warning for Aux 3 monitor	
	2	L-Aux 3 High Warning	Latched high warning for Aux 3 monitor	
	1	L-Aux 3 Low Alarm	Latched low alarm for Aux 3 monitor	
	0	L-Aux 3 High Alarm	Latched high alarm for Aux 3 monitor	
12	7-0	Reserved		
13	7-0	Custom		

1.7.2.4 Module-Level Monitors

Real time monitoring for the module includes temperature, supply voltage, auxiliary and vendor defined monitors as shown in Table 22.

The data format may facilitate greater resolution and range than required. Measurement accuracy is defined by the interoperability standard or module product specification.

Table 22- Module Monitors (Lower Page, active modules only)

Byte	Bit	Name	Description	Type
14	7-0	Module Monitor 1: Temperature MSB	Internally measured temperature: signed 2’s complement in 1/256 degree Celsius increments NOTE: Temp can be below 0.	RO Opt.
15	7-0	Module Monitor 1: Temperature1 LSB		
16	7-0	Module Monitor 2: Supply 3.3-volt MSB	Internally measured 3.3 volt input supply voltage: in 100 µV increments	RO Opt.
17	7-0	Module Monitor 2: Supply 3.3-volt LSB		
18	7-0	Module Monitor 3: Aux 1 MSB	TEC Current or Reserved monitor TEC Current: signed 2’s complement in 1/32767% increments of maximum TEC current +32767 is max TEC current (100%) – Max Heating -32767 is min TEC current (100%) – Max Cooling	RO Opt.
19	7-0	Module Monitor 3: Aux 1 LSB		
20	7-0	Module Monitor 4: Aux 2 MSB	TEC Current or Laser Temperature monitor TEC Current: signed 2’s complement in 1/32767% increments of maximum TEC current +32767 is max TEC current (100%) – Max Heating -32767 is min TEC current (100%) – Max Cooling Laser Temperature: signed 2’s complement in 1/256 degree Celsius increments	RO Opt.
21	7-0	Module Monitor 4: Aux 2 LSB		
22	7-0	Module Monitor 5: Aux 3 MSB	Laser Temperature or additional supply voltage monitor Laser Temperature: signed 2’s complement	RO Opt.

23	7-0	Module Monitor 5: Aux 3 LSB	in 1/256 degree Celsius increments Additional supply voltage monitor: in 100 µV increments	
24	7-0	Module Monitor 6: Custom MSB	Custom monitor	RO Opt.
25	7-0	Module Monitor 6: Custom LSB		

1.7.2.5 Module Global Controls

Module global controls are control aspects that are applicable to the entire module or all channels in the module. Channel-specific controls are located in Upper page 10h (Section 1.7.6.2).

Table 23- Module Global and Squelch Mode Controls (Lower Page, active modules only)

Byte	Bit	Name	Description	Type
26	7-6	Reserved		
	5	Squelch control	0b=Tx Squelch reduces OMA 1b=Tx Squelch reduces Pave (See Table 43)	RW Opt.
	4	ForceLowPwr	1b=Forces module into low power mode – see Section 1.4.2	RW RQD
	3	Software Reset	Self-clearing bit that causes the module to be reset. The effect is the same as asserting the reset pin for the appropriate hold time, followed by its de-assertion. This bit will be cleared to zero on a reset so a value of 0 will always be returned. 0b=not in reset 1b=Software reset	RW RQD
	2-0	Custom		
27-28	All	Reserved		
29-30	All	Custom	Custom Global controls	

1.7.2.6 Module-Level Flag Masks

The host may control which flags result in a hardware interrupt by setting masking bits in Table 24. The mask bits may be used to prevent continued interruption from on-going conditions, which would otherwise continually reassert the hardware interrupt signal. A mask bit is allocated for each flag bit.

A value of 1 in a masking bit prevents the assertion of the hardware interrupt signal, if one exists, by the corresponding latched flag bit. Masking bits are volatile: at power up or exit from module reset, all mask bits shall be clear.

Table 24- Module Level Flag Masks (Lower Page, active modules only)

Byte	Bits	Name	Description	Type
31	7-1	Reserved		RO
	0	Module State changed flag mask	Masking bit for Module State Changed flag	RW RQD
32	7	M-Vcc3.3 Low Warning flag mask	Masking bit for Vcc3.3 monitor low warning flag	RW Opt.
	6	M-Vcc3.3 High Warning flag mask	Masking bit for Vcc3.3 monitor high warning flag	

	5	M-Vcc3.3 Low Alarm flag mask	Masking bit for Vcc3.3 monitor low alarm flag	
	4	M-Vcc3.3 High Alarm flag mask	Masking bit for Vcc3.3 monitor high alarm flag	
	3	M-Temp Low Warning flag mask	Masking bit for temperature monitor low warning flag	
	2	M-Temp High Warning flag mask	Masking bit for temperature monitor high warning flag	
	1	M-Temp Low Alarm flag mask	Masking bit for temperature monitor low alarm flag	
	0	M-Temp High Alarm flag mask	Masking bit for temperature monitor high alarm flag	
33	7	M-Aux 2 Low Warning flag mask	Masking bit for Aux 2 monitor low warning flag	RW Opt.
	6	M-Aux 2 High Warning flag mask	Masking bit for Aux 2 monitor high warning flag	
	5	M-Aux 2 Low Alarm flag mask	Masking bit for Aux 2 monitor low alarm flag	
	4	M-Aux 2 High Alarm flag mask	Masking bit for Aux 2 monitor high alarm flag	
	3	M-Aux 1 Low Warning flag mask	Masking bit for Aux 1 monitor low warning flag	
	2	M-Aux 1 High Warning flag mask	Masking bit for Aux 1 monitor high warning flag	
	1	M-Aux 1 Low Alarm flag mask	Masking bit for Aux 1 monitor low alarm flag	
	0	M-Aux 1 High Alarm flag mask	Masking bit for Aux 1 monitor high alarm flag	
34	7	M-Vendor Defined Low Warning flag mask	Masking bit for Vendor defined low warning flag	RW Opt.
	6	M-Vendor Defined High Warning flag mask	Masking bit for Vendor defined high warning flag	
	5	M-Vendor Defined Low Alarm flag mask	Masking bit for Vendor defined low alarm flag	
	4	M-Vendor Defined High Alarm flag mask	Masking bit for Vendor defined high alarm flag	
	3	M-Aux 3 Low Warning flag mask	Masking bit for Aux 3 monitor low warning flag	
	2	M-Aux 3 High Warning flag mask	Masking bit for Aux 3 monitor high warning flag	
	1	M-Aux 3 Low Alarm flag mask	Masking bit for Aux 3 monitor low alarm flag	
	0	M-Aux 3 High Alarm flag mask	Masking bit for Aux 3 monitor high alarm flag	
35	7-0	Reserved flag mask		
36	7-0	Custom	Module level flag masks	

1.7.2.7 Application Advertising

Table 26 defines the module Application advertising fields. The Media Lane Assignment Options field for each Application is advertised in Table 47. See Section 1.5.2 for Application advertising methodology.

All modules shall advertise at least one Application. The first unused entry in Table 26 shall have FFh in the Host Electrical Code field to indicate the end of the list of supported Applications. Table 26 provides space for advertisement of up to eight Applications. If additional Applications need to be advertised, additional Application advertising fields are provided in Table 48.

Module Media Interface encodings are specified by module media interface tables in Appendix C. The Module Type Encoding field in Byte 85 is a required field that indicates which media interface table applies to the module. Valid module type encodings are specified in Table 25.

Table 25- Byte 85 Module Type Encodings

Code (Hex)	Module Type
00h	Undefined
01h	Optical Interfaces: MMF (see Table 79)
02h	Optical Interfaces: SMF (see Table 80)
03h	Passive Cu (see Table 81)
04h	Active Cables (see Table 82)
05h	BASE-T (see Table 83)
06h-3Fh	Reserved
40h-8Fh	Custom
90h-FFh	Reserved

Table 26- Application Advertising Fields (Lower page)

Byte	Bits	ApSel Code	Name	Description	Type
86	7-0	0001b	Host Electrical Interface Code	Code from Appendix C Table 78	RO RQD
87	7-0		Module Media Interface Code	Code from Appendix C Table 79-Table 83	
88	7-4		Host Lane Count	0000b=lane count defined by Application code 0001b=1 lane, 0010b=2 lanes.... 1000b=8 lanes. 1001b-1111b=reserved	
	3-0		Media Lane Count		
89	7-0		Host Lane Assignment Options (See Table 47 for Media Lane Assignment Options)	Bits 0-7 form a bit map and correspond to Host Lanes 1-8. A bit is coded 1 if the Application is allowed to begin on the corresponding host lane. Refer to Section 1.5.2 for details.	
90	7-0	0010b	Host Electrical Interface Code	Code from Appendix C Table 78	RO Opt.
91	7-0		Module Media Interface Code	Code from Appendix C Table 79-Table 83	
92	7-4		Host Lane Count	0000b=lane count defined by Application	

	3-0		Media Lane Count	code 0001b=1 lane, 0010b=2 lanes.... 1000b=8 lanes. 1001b-1111b=reserved	
93	7-0		Host Lane Assignment Options (See Table 47 for Media Lane Assignment Options)	Bits 0-7 form a bit map and correspond to Host Lanes 1-8. A bit is coded 1 if the Application is allowed to begin on the corresponding host lane. Refer to Section 1.5.2 for details.	
94	7-0	0011b	Host Electrical Interface Code	Code from Appendix C Table 78	RO Opt.
95	7-0		Module Media Interface Code	Code from Appendix C Table 79-Table 83	
96	7-4		Host Lane Count	0000b=lane count defined by Application code 0001b=1 lane, 0010b=2 lanes.... 1000b=8 lanes. 1001b-1111b=reserved	
	3-0		Media Lane Count		
97	7-0		Host Lane Assignment Options (See Table 47 for Media Lane Assignment Options)	Bits 0-7 form a bit map and correspond to Host Lanes 1-8. A bit is coded 1 if the Application is allowed to begin on the corresponding host lane. Refer to Section 1.5.2 for details.	
98	7-0	0100b	Host Electrical Interface Code	Code from Appendix B Table 78	RO Opt.
99	7-0		Module Media Interface Code	Code from Appendix C Table 79-Table 83	
100	7-4		Host Lane Count	0000b=lane count defined by Application code 0001b=1 lane, 0010b=2 lanes.... 1000b=8 lanes. 1001b-1111b=reserved	
	3-0		Media Lane Count		
101	7-0		Host Lane Assignment Options (See Table 47 for Media Lane Assignment Options)	Bits 0-7 form a bit map and correspond to Host Lanes 1-8. A bit is coded 1 if the Application is allowed to begin on the corresponding host lane. Refer to Section 1.5.2 for details.	
102	7-0	0101b	Host Electrical Interface Code	Code from Appendix C Table 78	RO Opt.
103	7-0		Module Media Interface Code	Code from Appendix C Table 79-Table 83	
104	7-4		Host Lane Count	0000b=lane count defined by Application code 0001b=1 lane, 0010b=2 lanes.... 1000b=8 lanes. 1001b-1111b=reserved	
	3-0		Media Lane Count		
105	7-0		Host Lane Assignment Options (See Table 47 for Media Lane Assignment Options)	Bits 0-7 form a bit map and correspond to Host Lanes 1-8. A bit is coded 1 if the Application is allowed to begin on the corresponding host lane. Refer to Section 1.5.2 for details.	
106	7-0	0110b	Host Electrical Interface Code	Code from Appendix C Table 78	RO Opt.
107	7-0		Module Media Interface Code	Code from Appendix C Table 79-Table 83	

108	7-4		Host Lane Count	0000b=lane count defined by Application code 0001b=1 lane, 0010b=2 lanes.... 1000b=8 lanes. 1001b-1111b=reserved	
	3-0		Media Lane Count		
109	7-0		Host Lane Assignment Options (See Table 47 for Media Lane Assignment Options)	Bits 0-7 form a bit map and correspond to Host Lanes 1-8. A bit is coded 1 if the Application is allowed to begin on the corresponding host lane. Refer to Section 1.5.2 for details.	
110	7-0	0111b	Host Electrical Interface Code	Code from Appendix C Table 78	RO Opt.
111	7-0		Module Media Interface Code	Code from Appendix C Table 79-Table 83	
112	7-4		Host Lane Count	0000b=lane count defined by Application code 0001b=1 0010b=2 lanes.... 1000b=8 lanes. 1001b-1111b=reserved	
	3-0		Media Lane Count		
113	7-0		Host Lane Assignment Options (See Table 47 for Media Lane Assignment Options)	Bits 0-7 form a bit map and correspond to Host Lanes 1-8. A bit is coded 1 if the Application is allowed to begin on the corresponding host lane. Refer to Section 1.5.2 for details.	
114	7-0	1000b	Host Electrical Interface Code	Code from Appendix C Table 78	RO Opt.
115	7-0		Module Media Interface Code	Code from Appendix C Table 79-Table 83	
116	7-4		Host Lane Count	0000b=lane count defined by Application code 0001b=1 lane, 0010b=2 lanes.... 1000b=8 lanes. 1001b-1111b=reserved	
	3-0		Media Lane Count		
117	7-0		Host Lane Assignment Options (See Table 47 for Media Lane Assignment Options)	Bits 0-7 form a bit map and correspond to Host Lanes 1-8. A bit is coded 1 if the Application is allowed to begin on the corresponding host lane. Refer to Section 1.5.2 for details.	

1.7.2.8 Password Entry and Change

Bytes 118-125 are reserved for the password entry function. The Password entry bytes may be write only and will be retained until power down, reset, or rewritten by host. This function is used to control write access to the custom page 03h (EEPROM) and other custom upper pages. Additionally, module vendors may use this function to implement write protection of Serial ID and other read only information. Note that multiple module manufacturer passwords may be defined to allow selective access to write to various sections of memory.

Password access shall not be required to read memory map data in lower Page 00h or in Upper Page 00h, 01h, 02h, 03h, 10h or 11h. Host manufacturer and module manufacturer passwords shall be distinguished by the high order bit (bit 7, Byte 122). All host manufacturer passwords shall fall in the range of 00000000h to 7FFFFFFFh, and all module manufacturer passwords in the range of 80000000h to FFFFFFFFh. Host system manufacturer passwords shall be initially set to 00001011h in new modules.

Host manufacturer passwords may be changed by writing a new password in Bytes 118-121 when the correct current module manufacturer password has been entered in Bytes 122-125, with the high order bit being ignored and forced to a value of 0 in the new password. The password entry field shall be set to 00000000h on power up and reset.

1.7.2.9 Bank Select Byte

The value written to the Bank Select byte 126 determines which bank is accessed when banking is supported. The module shall ignore the Bank Select byte if the Page Select byte is less than 10h. The Bank Select byte shall also be ignored if the memory map address being accessed is less than or equal to 127. Writing the value of a non-supported bank shall not be accepted by the module. In this case the Bank Select byte shall revert to bank 0 and read/write operations shall be to bank 0. Note: the host should write the Page and Bank Select in 1 byte writes.

1.7.2.10 Page Select Byte

The value written to the Page Select byte 127 determines which upper page is accessed. A value of 00h indicates upper memory Page 00h is mapped to Bytes 128-255 and a value of 01h indicates that upper Page 01h if available is mapped to Bytes 128-255. Similarly, values of 02h, 03h, etc., indicate that the upper page identified is mapped to Bytes 128-255. Writing the value of a non-supported page shall not be accepted by the module. In such cases the Page Select byte shall revert to 0 and read/write operations shall be to upper page 00h. Note: the host should write the Page and Bank Select in 1 byte writes.

1.7.3 Upper Page 00h

Upper page 00h contains static read-only module identification information. Upper page 00h shall be implemented for both paged and flat memory implementations and is required for all modules and cable assemblies.

Table 27- Upper Page 00 Overview (Page 00h)

Address	Size (bytes)	Name	Description
128	1	Identifier	Identifier Type of module
129-144	16	Vendor name	Vendor name (ASCII)
145-147	3	Vendor OUI	Vendor IEEE company ID
148-163	16	Vendor PN	Part number provided by vendor (ASCII)
164-165	2	Vendor rev	Revision level for part number provided by vendor (ASCII)
166-181	16	Vendor SN	Vendor Serial Number (ASCII)
182-189	8	Date Code	
190-199	10	CLEI code	Common Language Equipment Identification code
200-201	2	Module power characteristics	
202	1	Cable assembly length	
203	1	Media Connector Type	
204-209	6	Copper Cable Attenuation	
210-211	2	Cable Assembly Lane Information	
212	1	Media Interface Technology	
213-220	8	Reserved	
221	1	Custom	
222	1	Checksum	Includes bytes 128-221
223-255	33	Custom Info NV	

1.7.3.1 Identifier

The identifier value specifies the physical device implementation and, by inference, memory map data format. This field should contain the same value as byte 0 in the lower page. These values are maintained in the Transceiver Management section of SFF-8024.

Table 28- Identifiers (Page 00h)

Byte	Bits	Name	Description	Type
128	7-0	Identifier	Identifier - Type of Serial Module - See SFF-8024.	RO RQD

1.7.3.2 Vendor Name (Page 00h, Bytes 129-144, RO, required)

The vendor name is a required 16 character field (bytes 129-144) that contains ASCII characters, left aligned and padded on the right with ASCII spaces (20h). The vendor name shall be the full name of the corporation, a commonly accepted abbreviation of the name of the corporation, the SCSI company code for the corporation, or the stock exchange code for the corporation. The vendor name may be the original manufacturer of the module or the name of the module reseller. In both cases, the Vendor Name and Vendor OUI (if specified) shall correlate to the same company. At least one of the vendor name or the vendor OUI fields shall contain valid serial data.

1.7.3.3 Vendor Organizationally Unique Identifier (Page 00h, Bytes 145-147, RO, required)

The vendor organizationally unique identifier field (vendor OUI) is a required 3-byte field (bytes 145-147) that contains the IEEE Company Identifier for the vendor. A value of all zero in the 3-byte field indicates that the Vendor OUI is unspecified.

1.7.3.4 Vendor Part Number (Page 00h, Bytes 148-163, RO, required)

The vendor part number (vendor PN) is a required 16-byte field (bytes 148-163) that contains ASCII characters, left aligned and padded on the right with ASCII spaces (20h), defining the vendor part number or product name. A value of all zero in the 16-byte field indicates that the vendor part number is unspecified.

1.7.3.5 Vendor Revision Number (Page 00h, Bytes 164-165, RO, required)

The vendor revision number (vendor rev) is a required 2-byte field (bytes 164-165) that contains ASCII characters, left aligned and padded on the right with ASCII spaces (20h), defining the vendor’s product revision number. A value of all zero in the field indicates that the vendor Rev is unspecified.

1.7.3.6 Vendor Serial Number (Page 00h, Bytes 166-181, RO, required)

The vendor serial number (vendor SN) is a required 16-character field (bytes 166-181) that contains ASCII characters, left aligned and padded on the right with ASCII spaces (20h), defining the vendor’s serial number for the Product. A value of all zero in the 16-byte field indicates that the vendor serial number is unspecified.

1.7.3.7 Date Code

The date code is an 8-byte field that contains the vendor’s date code in ASCII characters. The date code is mandatory. The date code shall be in the following format:

Table 29- Date Code (Page 00h)

Byte	Bits	Name	Description	Type
182-183	All	Date code year	ASCII code, two low order digits of year (00=2000)	RO RQD
184-185	All	Date code month	ASCII code digits of month (01=Jan through 12=Dec)	RO RQD
186-187	All	Date code day of month	ASCII code day of month (01-31)	RO RQD
188-189	All	Lot code	ASCII code, custom lot code, may be blank	RO Opt.

1.7.3.8 CLEI Code

The CLEI (Common Language Equipment Identification) code is a 10-byte field (bytes 190-199) that contains the vendor’s CLEI code in ASCII characters. The CLEI code is optional.

1.7.3.9 Module Power Characteristics

The module power characteristics are defined in the two memory locations in Table 30. The power class identifier and max power field both specify maximum power dissipation over operating conditions and lifetime with all supported settings set to worst case values. See Section 1.4.2 for details.

Table 30- Module Power Class and Max Power (Page 00h)

Byte	Bits	Name	Description	Type
200	7-5	Module Card Power Class[1]	000: Power class 1 001: Power class 2 010: Power class 3 011: Power class 4 100: Power class 5 101: Power class 6 110: Power class 7 111: Power class 8 (see byte 201)	RO RQD
	4-0	Reserved		RO
201	7-0	Max Power	Maximum power consumption in multiples of 0.25 W rounded up to the next whole multiple of 0.25 W	RO RQD

Note 1: See hardware specification for Power class values

1.7.3.10 Cable Assembly Length

The link length field provides the physical interconnect length of cable assemblies, including both passive copper and active optical or electrical cables. Transceivers with separable optical connectors shall populate this field with a 0. The code 11111111b means that the device supports a link length greater than 6300 m.

Table 31- Cable Assembly Length (Page 00h)

Byte	Bits	Name	Description	Type
202	7-6	Length multiplier field (Copper or active cable)	Multiplier for value in bits 5-0. 00 = multiplier of 0.1 01 = multiplier of 1 10 = multiplier of 10 11 = multiplier of 100	RO RQD
	5-0	Base Length field (copper of active cable)	Link length base value in meters. To calculate actual link length use multiplier in bits 7-6.	

1.7.3.11 Media Connector Type

The Connector Type field indicates the connector type for the media side of the module. These values are maintained in the Connector References section of SFF-8024.

Table 32- Media Connector Type (Page 00h)

Byte	Bits	Name	Description	Type
203	7-0	Connector Type	Type of connector present in the module. See SFF-8024 for codes.	RO RQD

1.7.3.12 Copper Cable Attenuation

These Bytes are used to define the cable attenuation for passive copper cables. For transceiver modules bytes 204-209 are reserved.

Table 33- Copper Cable Attenuation (Page 00h)

Byte	Bits	Name	Description	Type
204	7-0	5 GHz attenuation	Passive copper cable attenuation at 5 GHz in 1 dB increments	RO Opt.
205	7-0	7 GHz attenuation	Passive copper cable attenuation at 7 GHz in 1 dB increments	RO Opt.
206	7-0	12.9 GHz attenuation	Passive copper cable attenuation at 12.9 GHz in 1 dB increments	RO Opt.
207	7-0	25.8 GHz attenuation	Passive copper cable attenuation at 25.8 GHz in 1 dB increments	RO Opt.
208-209	All	reserved		RO

1.7.3.13 Cable Assembly Lane Information

Table 34 (Byte 210) is applied to all modules to indicate the number of near end media lanes implemented. With optical modules a media lane may be a fiber or a wavelength. Far end cable lane group fields (Byte 211) are used for cable assemblies to indicate the number of far end lanes implemented and the far end lane configuration. Far end cable lane group fields do not apply to modules with detachable media connectors. No information is given on the type of module on the far end of the cable (i.e. QSFP, SFP etc.), only the number of modules in the far end.

Table 34- Media lane interface implementation (Page 00h)

Byte	Bits	Name	Description	Type
210	7	Near end implementation lane 8	0b=Lane 8 implemented in near end 1b=Lane 8 not implemented in near end	RO Opt.
	6	Near end implementation lane 7	0b=Lane 7 implemented in near end 1b=Lane 7 not implemented in near end	
	5	Near end implementation lane 6	0b=Lane 6 implemented in near end 1b=Lane 6 not implemented in near end	
	4	Near end implementation lane 5	0b=Lane 5 implemented in near end 1b=Lane 5 not implemented in near end	
	3	Near end implementation lane 4	0b=Lane 4 implemented in near end 1b=Lane 4 not implemented in near end	
	2	Near end implementation lane 3	0b=Lane 3 implemented in near end 1b=Lane 3 not implemented in near end	
	1	Near end implementation lane 2	0b=Lane 2 implemented in near end 1b=Lane 2 not implemented in near end	
	0	Near end implementation lane 1	0b=Lane 1 implemented in near end 1b=Lane 1 not implemented in near end	
211	7-5	Reserved		RO
	4-0	Far End Configuration	See Table 35 for config code of discrete far end connectors	RO Opt.

Table 35 contains codes for all near end supported combinations of far end modules (lane groups a to h), and maps those far end modules (lane groups) to the connected near end lane number. Unique letters indicate discrete modules. Note that the discrete modules may or may not be the same module type.

Table 35- Far end cable lane groups advertising codes (Page 00h)

Far End Cable Lane Groups Advertising Codes									
Config Code		Near End Host Lane Number							
Decimal	Binary	1	2	3	4	5	6	7	8
0	00000	Undefined - Use for detachable modules							
1	00001	a	b	c	d	e	f	g	h
2	00010	a	a	a	a	a	a	a	a
3	00011	a	a	a	a	e	e	e	e
4	00100	a	b	c	d	e	e	e	e
5	00101	a	b	c	c	e	e	e	e
6	00110	a	a	c	d	e	e	e	e
7	00111	a	a	c	c	e	e	e	e
8	01000	a	a	a	a	e	f	g	h
9	01001	a	a	a	a	e	f	g	g
10	01010	a	a	a	a	e	e	g	h
11	01011	a	a	a	a	e	e	g	g
12	01100	a	a	c	c	e	e	g	g
13	01101	a	b	c	c	e	e	g	g
14	01110	a	a	c	d	e	e	g	g
15	01111	a	b	c	d	e	e	g	g
16	10000	a	a	c	c	e	f	g	g
17	10001	a	b	c	c	e	f	g	g
18	10010	a	a	c	d	e	f	g	g
19	10011	a	b	c	d	e	f	g	g
20	10100	a	a	c	c	e	e	g	h
21	10101	a	b	c	c	e	e	g	h
22	10110	a	a	c	d	e	e	g	h
23	10111	a	b	c	d	e	e	g	h
24	11000	a	a	c	c	e	f	g	h
25	11001	a	b	c	c	e	f	g	h
26	11010	a	a	c	d	e	f	g	h
27-31	11011-11111	reserved							

1.7.3.14 Media Interface Technology (required)

Byte 212 is a required byte that defines aspects of the device or cable technology, using the encodings in Table 36. An active optical cable may distinguish from a separable module using Byte 203 (see Section 1.7.3.11).

Table 36- Media Interface Technology encodings

Code	Description of physical device
00h	850 nm VCSEL
01h	1310 nm VCSEL
02h	1550 nm VCSEL
03h	1310 nm FP
04h	1310 nm DFB
05h	1550 nm DFB
06h	1310 nm EML
07h	1550 nm EML
08h	Others
09h	1490 nm DFB
0Ah	Copper cable unequalized
0Bh	Copper cable passive equalized
0Ch	Copper cable, near and far end limiting active equalizers
0Dh	Copper cable, far end limiting active equalizers
0Eh	Copper cable, near end limiting active equalizers
0Fh	Copper cable, linear active equalizers
10h-ffh	Reserved

1.7.3.15 Checksum

The check code is a one byte code that can be used to verify that the read-only static data on Page 00h is valid. The check code shall be the low order 8 bits of the sum of the contents of all the bytes from byte 128 to byte 221, inclusive.

1.7.3.16 Custom Info (non-volatile)

Bytes 223-255 are allocated in the non-volatile storage space for information provided by the original manufacturer of the module or the module reseller. This information persists across module reset and power cycle. The contents of this area are not defined by this specification.

1.7.4 Upper Page 01h

Upper Page 01h contains advertising fields that define properties that are unique to active modules and cable assemblies. The presence of Upper Page 01h is advertised in bit 7 in Page 00h byte 2. All fields on Upper Page 01h are read-only and static.

Table 37- Upper Page 01 Overview (Page 01h)

Byte	Size (bytes)	Name	Description
128-131	4	Module Firmware and Hardware revisions	
132-137	6	Supported link length	Supported lengths of various fiber media
138-139	2	Nominal Wavelength	
140-141	2	Wavelength Tolerance	
142-144	3	Implemented Management Interface features advertising	
145-154	10	Module Characteristics advertising	
155-156	2	Implemented Controls advertising	

157-158	2	Implemented Flags advertising	
159-160	2	Implemented Monitors advertising	
161-162	2	Implemented Signal Integrity Controls advertising	
163-175	13	Reserved	
176-190	15	Module Media Lane advertising	
191-222	32	Custom	
223-250	28	Extended Module Host-Media Interface Advertising options	
251-254	4	Reserved	
255	1	Checksum	Checksum of bytes 130-254[1]

Note 1: The firmware version bytes 128-129 are excluded from the checksum to allow module implementers to programmatically generate these fields and avoid requiring a memory map update when firmware is updated.

1.7.4.1 Module Firmware and Hardware Revisions

The module hardware and firmware major and minor revision shall be reported in these fields. The finished module or cable assembly revision number shall be reported in the Vendor Revision Number field described in section 1.7.3.5.
Table 38describes the memory map locations for module firmware and hardware revisions. The module firmware major and minor revisions shall be represented as numeric values. These two values shall not be included in the Page 01h checksum. The module hardware major and minor revisions shall be represented as numeric values. These two values shall be included in the Page 01h checksum.

Table 38- Module Firmware and Hardware Revisions (Page 01h)

Byte	Bits	Name	Description	Type
128	7-0	Module firmware major revision	Numeric representation of module firmware major revision	RO RQD
129	7-0	Module firmware minor revision	Numeric representation of module firmware minor revision	RO RQD
130	7-0	Module hardware major revision	Numeric representation of module hardware major revision	RO RQD
131	7-0	Module hardware minor revision	Numeric representation of module hardware minor revision	RO RQD

1.7.4.2 Supported Link Length

These bytes define the maximum supported fiber media length for each type of fiber media at the maximum module-supported bit rate for active modules with a separable optical interface. Unsupported media types shall be populated with zeroes. Active optical cables shall populate the fields in this table with zeroes and instead report their actual length using the fields in Table 31.

Table 39- Supported Fiber Link Length (Page 01h)

Byte	Bits	Name	Description	Type
132	7-6	Length multiplier(SMF)	Link length multiplier for SMF fiber 00 = 0.1 (1 to 6.3 km) 01 = 1 (1 to 63 km) 10, 11 = reserved	RO RQD
	5-0	Base Length (SMF)	Base link length for SMF fiber. Must be multiplied by value in bits 7-6 to calculate actual link length in km.	
133	7-0	Length (OM5)	Link length supported for OM5 fiber, units of 2m (2 to 510 m)	RO RQD
134	7-0	Length (OM4)	Link length supported for OM4 fiber, units of 2m (2 to 510 m)	RO RQD
135	7-0	Length (OM3)	Link length supported for EBW 50/125 µm fiber (OM3), units of 2m (2 to 510 m)	RO RQD
136	7-0	Length (OM2)	Link length supported for 50/125 µm fiber (OM2), units of 1m (1 to 255 m)	RO RQD
137	7-0	Reserved		RORQD

The link length supported for SMF fiber specifies the link length that is supported by the device while operating in compliance with the applicable standards using single mode fiber. The supported link length is as specified in the SFF 8074i standard. The value is in units of kilometers.

The link length supported for OM5 fiber specifies the link length that is supported by the device while operating in compliance with the applicable standards using 4700 MHz*km (850 nm) and 2470 MHz*km (953 nm) extended bandwidth 50 micron core multimode fiber. The value is in units of two meters.

The link length supported for OM4 fiber specifies the link length that is supported by the device while operating in compliance with the applicable standards using 4700 MHz*km (850 nm) extended bandwidth 50 micron core multimode fiber. The value is in units of two meters.

The link length supported for OM3 fiber specifies the link length that is supported by the device while operating in compliance with the applicable standards using 2000 MHz*km (850 nm) extended bandwidth 50 micron core multimode fiber. The value is in units of two meters.

The link length supported for OM2 fiber specifies the link length that is supported by the device while operating in compliance with the applicable standards using 500 MHz*km (850 nm and 1310 nm) 50 micron multi-mode fiber. The value is in units of one meter.

1.7.4.3 Wavelength (Page 01h, Bytes 138 - 139, RO, Required)

The wavelength field specifies the nominal transmitter output wavelength at room temperature; this is a 16-bit value with byte 138 as the high order byte and byte 139 as the low order byte. The laser wavelength value is equal to the 16-bit integer value of the wavelength in nm divided by 20 (units of 0.05nm). This resolution should be adequate to cover all relevant wavelengths yet provide enough resolution for all expected Applications. For accurate representation of controlled wavelength Applications, this value should represent the center of the guaranteed wavelength range.

1.7.4.4 Wavelength Tolerance (Page 01h, Bytes 140 - 141, RO, Required)

The wavelength tolerance is the worst case +/- range of the transmitter output wavelength under all normal operating conditions; this is a 16-bit value with byte 140 as the high order byte and byte 141 as the low order byte. The laser wavelength tolerance is equal to the 16-bit integer value in nm divided by 200 (units of 0.005nm). Thus, the following two examples:

Example 1:
10GBASE-LR Wavelength Range = 1260 to 1355 nm
Nominal Wavelength in bytes 138 - 139 = 1307.5 nm.
Represented as INT (1307.5 nm * 20) = 26150 = 6626h
Wavelength Tolerance in bytes 140 - 141 = 47.5nm.
Represented as INT (47.5 nm * 200) = 9500 = 251Ch

Example 2:
ITU-T Grid Wavelength = 1534.25 nm with 0.236 nm Tolerance
Nominal Wavelength in bytes 138 - 139 = 1534.25 nm.
Represented as INT (1534.25nm * 20) = 30685 = 77DDh
Wavelength Tolerance in bytes 140 - 141 = 0.236 nm.
Represented as INT (0.236 nm * 200) = 47 = 002Fh

1.7.4.5 Implemented Memory Pages and Durations Advertising

The fields in Table 40 advertise module implementation of optional management interface features.

The ModSelL wait time fields define the required setup time for the ModSelL signal after the host asserts a low level on ModSelL before the start of a two-wire serial bus transaction, and the required delay from completion of a two-wire serial bus transaction before the host can de-assert the ModSelL signal. For example, if the module wait time is 1.6ms, the mantissa field (bits 4-0) will be 11001b and the exponent field (bits 7-5) will be 110b indicating six zeros after the 11001b for a net result of 11001000000b or 1600 decimal.

Table 40- Implemented Management Interface Features Advertising (Page 01h)

Byte	Bit	Name	Description	Type
142	7-6	Reserved		RORQD
	5	Diagnostic pages implemented	Bank page 1Ch-1Dh implemented for diagnostic features	RO RQD
	4	reserved		
	3	reserved		
	2	Page 03h implemented	Indicates User page 03h implemented	
	1-0	Implemented Banks	Indicates bank pages implemented for pages 10h-1Fh 00b=bank 0 implemented 01b=banks 0 and 1 implemented 10b, 11b=reserved	
143	7-5	ModSelL wait time exponent	The ModSelL wait time value is the mantissa x 2^exponent expressed in micro-seconds. In other words, the mantissa field is shifted up by the number of bits indicated in the exponent field (time = mantissa << exponent)	RO Opt.
	4-0	ModSelL wait time mantissa		
144	7-4	DataPathDeinit_MaxDuration or ModulePwrDn_MaxDuration	Encoded maximum duration of the DataPathDeinit or ModulePwrDn state whichever is greater (see Table 41)	RO RQD
	3-0	DataPathInit_MaxDuration	Encoded maximum duration of the DataPathInit state (see Table 41)	

The DataPathInit_MaxDuration and DataPathDeinit_MaxDuration fields are defined so host implementers can determine when something has gone wrong in the module during these states, for example a module firmware hang. These values should be selected to represent the worst-case durations of these two states, across all advertised Applications and combinations of data paths. See sections 1.5.3.2 and 1.5.3.4 for details of the DataPathInit and DataPathDeinit states.

Table 41- State Duration Encoding (Page 01h)

Encoding	Maximum State Duration
0000b	Maximum state duration is less than 1 ms
0001b	1 ms <= maximum state duration < 5 ms
0010b	5 ms <= maximum state duration < 10 ms
0011b	10 ms <= maximum state duration < 50 ms
0100b	50 ms <= maximum state duration < 100 ms
0101b	100 ms <= maximum state duration < 500 ms
0110b	500 ms <= maximum state duration < 1 s
0111b	1 s <= maximum state duration < 5 s
1000b	5 s <= maximum state duration < 10 s
1001b	10 s <= maximum state duration < 1 min
1010b	1 min <= maximum state duration < 5 min
1011b	5 min <= maximum state duration < 10 min
1100b	10 min <= maximum state duration < 50 min
1101b	Maximum state duration >= 50 min
1110b	Reserved
1111b	Reserved

1.7.4.6 Module Characteristics Advertising

The fields in Table 42 describe the characteristics of certain module properties. Some features may be optional. Advertisement of the implementation of optional features is in sections 1.7.4.7 through 1.7.4.10. A Tx synchronous group is defined as a Tx input lane or group of TX input lanes sourced from the same clock domain. Two different Tx synchronous groups may be sourced from different clock domains. There may be a limit on the maximum permissible clock tolerance between two different Tx synchronous groups, as defined by the industry standard associated with a given application code. Refer to applicable industry standards.

A Tx synchronous group can contain one or more data paths, as long as the Tx lanes on all data paths are sourced from the same clock domain and the module takes measures to ensures that active data paths continue to operate undisturbed even as other data paths (and their associated Tx input lanes) are enabled/disabled by the host.

Table 42- Module Characteristics Advertising (Page 01h)

Byte	Bit	Name	Description	Type
145	7	Cooling implemented	0b=Uncooled transmitter device 1b=Cooled transmitter	RO RQD
	6-5	Tx input clock recovery capabilities	00b=module requires all Tx input lanes to be in a single Tx synchronous group 01b=module allows Tx input lanes 1-4 and 5-8 to be in separate Tx synchronous groups 10b=module allows Tx input lanes 1-2, 3-4, 5-6, 7-8 to be in separate Tx synchronous groups 11b=module allows each Tx input lane to be in a separate Tx synchronous group	RO RQD
	4-3	Reserved		RO
	2	Aux 3 Monitor type	1b=Aux 3 monitor is Vcc2 0b=Aux 3 monitor is Laser Temperature	RO Opt.
	1	Aux 2 Monitor type	1b=Aux 2 monitor is TEC current 0b=Aux 2 monitor is Laser Temperature	RO Opt.
	0	Aux 1 Monitor type	1b=Aux 1 monitor is TEC current 0b=Aux 1 monitor is reserved	RO Opt.
146	7-0	Maximum module temperature	Maximum allowed module case temperature 8-bit signed 2's complement value in 1 deg C increments. A value of all zeroes indicates not specified.	RO Opt.
147	7-0	Minimum module temperature	Minimum allowed module case temperature 8-bit signed 2's complement value in 1 deg C increments. A value of all zeroes indicates not specified.	RO Opt.
148	7-0	Propagation Delay MSB	Propagation delay of the non-separable AOC in multiples of 10 ns rounded to the nearest 10 ns. A value of all zeroes indicates not specified.	RO Opt.
149	7-0	Propagation Delay LSB		RO Opt.
150	7-0	Minimum operating voltage	Minimum supported module operating voltage, in 20 mV increments (0 - 5.1 V) A value of all zeroes indicates not specified.	RO Opt.
151	7	Detector type	0b=PIN detector 1b=APD detector	RO RQD
	6-5	RX Output Eq type	00b=Peak-to-peak amplitude stays constant, or not implemented, or no information 01b=Steady-state amplitude stays constant 10b=Average of peak-to-peak and steady-state amplitude stays constant 11b=Reserved	
	4	Rx Optical Power Measurement type	0b=OMA 1b=average power	
	3	Rx LOS type	0b=Rx LOS responds to OMA 1b=Rx LOS responds to Pave	
	2	Rx LOS fast mode implemented	0b=Rx LOS fast mode not implemented 1b=Rx LOS fast mode implemented Refer to form factor hardware specification for timing requirements	
	1	Tx Disable fast mode implemented	0b=Tx Disable fast mode not implemented 1b=Tx Disable fast mode implemented Refer to form factor hardware specification for timing requirements	
	0	Module-Wide Tx Disable	0b=Tx Disable implemented per lane 1b=Any Tx Disable control bit being set disables all Tx lanes	
152	7-0	Per lane CDR Power	Minimum power consumption saved per CDR per lane	RO

Byte	Bit	Name	Description	Type
		saved	when placed in CDR bypass in multiples of 0.01 W rounded up to the next whole multiple of 0.01 W	Opt.
153	7	Rx Output Amplitude code 0011b implemented[1]	0b=Amplitude code 0011b not implemented 1b=Amplitude code 0011b implemented	RO Opt.
	6	Rx Output Amplitude code 0010b implemented[1]	0b=Amplitude code 0010b not implemented 1b=Amplitude code 0010b implemented	
	5	Rx Output Amplitude code 0001b implemented[1]	0b=Amplitude code 0001b not implemented 1b=Amplitude code 0001b implemented	
	4	Rx Output Amplitude code 0000b implemented[1]	0b=Amplitude code 0000b not implemented 1b=Amplitude code 0000b implemented	
	3-0	Max Tx Input Eq	Maximum supported value of the Tx Input Equalization control for manual/fixed programming. (see Table 12)	
154	7-4	Max Rx Output Eq Post-cursor	Maximum supported value of the Rx Output Eq Post-cursor control. (see Table 13)	RO Opt.
	3-0	Max Rx Output Eq Pre-cursor	Maximum supported value of the Rx Output Eq Pre-cursor control (see Table 13)	

Note 1: See Table 14

1.7.4.7 Implemented Controls Advertisement

Table 43 describes implemented module and lane controls.

Table 43- Implemented Controls Advertisement (Page 01h)

Byte	Bit	Name	Description	Type
155	7	Wavelength control implemented	0b=No wavelength control 1b=Active wavelength control implemented	RO RQD
	6	Tunable transmitter implemented	0b=Transmitter not tunable 1b=Transmitter tunable	
	5-4	Tx Squelch implemented	00b=Tx Squelch not implemented 01b=Tx Squelch reduces OMA 10b=Tx Squelch reduces Pave 11b=User control, both OMA and Pave squelch supported. (see Table 23)	
	3	Tx Force Squelch implemented	0b=Tx Force Squelch not implemented 1b=Tx Force Squelch implemented	
	2	Tx Squelch Disable implemented	0b=Tx Squelch Disable not implemented 1b=Tx Squelch Disable implemented	
	1	Tx Disable implemented	0b=Tx Disable not implemented 1b=Tx Disable implemented	
	0	Tx Polarity Flip implemented	0b=Tx Polarity Flip not implemented 1b=Tx Polarity Flip implemented	
156	7-3	Reserved		RORQD
	2	Rx Squelch Disable implemented	0b=Rx Squelch Disable not implemented 1b=Rx Squelch Disable implemented	RO RQD
	1	Rx Disable implemented	0b=Rx Disable not implemented 1b=Rx Disable implemented	
	0	Rx Polarity Flip implemented	0b=Rx Polarity Flip not implemented 1b=Rx Polarity Flip implemented	

1.7.4.8 Implemented Flags Advertisement

Table 44 describes implemented module and lane flags.

Table 44- Implemented Flags Advertisement (Page 01h)

Byte	Bit	Name	Description	Type
157	7-4	Reserved		RO RQD
	3	Tx Adaptive Input Eq Fault flag implemented	0b=Tx Adaptive Input Eq Fault flag not implemented 1b=Tx Adaptive Input Eq Fault flag implemented	RO RQD
	2	Tx CDR LOL flag implemented	0b=Tx CDR Loss of Lock flag not implemented 1b=Tx CDR Loss of Lock flag implemented	
	1	Tx LOS flag implemented	0b=Tx Loss of Signal flag not implemented 1b=Tx Loss of Signal flag implemented	
	0	Tx Fault flag implemented	0b=Tx Fault flag not implemented 1b=Tx Fault flag implemented	
158	7-3	Reserved		RO RQD
	2	Rx LOL flag implemented	0b=Rx CDR Loss of Lock flag not implemented 1b=Rx CDR Loss of Lock flag implemented	RO RQD
	1	Rx LOS flag implemented	0b=Rx Loss of Signal flag not implemented 1b=Rx Loss of Signal flag implemented	
	0	Reserved		RO

1.7.4.9 Implemented Monitors Advertisement

Table 45 describes implemented module and lane monitors.

Table 45- Implemented Monitors Advertisement (Page 01h)

Byte	Bit	Name	Description	Type
159	7-6	Reserved		RO RQD
	5	Custom monitor implemented	0b=Custom monitor not implemented 1b=Custom monitor implemented	RO RQD
	4	Aux 3 monitor implemented	0b=Aux 3 monitor not implemented 1b=Aux 3 monitor implemented	
	3	Aux 2 monitor implemented	0b=Aux 2 monitor not implemented 1b=Aux 2 monitor implemented	
	2	Aux 1 monitor implemented	0b=Aux 1 monitor not implemented 1b=Aux 1 monitor implemented	
	1	Internal 3.3 Volts monitor implemented	0b=Internal 3.3 V monitor not implemented 1b=Internal 3.3 V monitor implemented	
	0	Temperature monitor implemented	0b=Temperature monitor not implemented 1b=Temperature monitor implemented	
160	7-5	Reserved		RO RQD
	4-3	Tx Bias current measurement and threshold multiplier	Multiplier for 2uA Bias current increment used in Tx Bias current monitor and threshold registers (see Table 51 and Table 70) 00b=multiply x1 01b=multiply x2 10b=multiply x4 11b=reserved	

	2	Rx Optical Input Power monitor implemented	0b=Rx Optical Input Power monitor not implemented 1b=Rx Optical Input Power monitor implemented	
	1	Tx Output Optical Power monitor implemented	0b=Tx Output Optical Power monitor not implemented 1b=Tx Output Optical Power monitor implemented	
	0	Tx Bias monitor implemented	0b=Tx Bias monitor not implemented 1b=Tx Bias monitor implemented	

1.7.4.10 Implemented Signal Integrity Controls

Table 46 describes the implemented signal integrity controls.

Table 46- Implemented Signal Integrity Controls (Page 01h)

Byte	Bit	Name	Description	Type
161	7	Reserved		RO RQD
	6-5	Tx Input Eq Store/Recall buffer count	00b=Tx Input Eq Store/Recall not implemented 01b=Tx Input Eq Store/Recall buffer count=1 10b=Tx Input Eq Store/Recall buffer count=2 11b=reserved	RO RQD
	4	Tx Input Eq Freeze implemented	0b=Tx Input Eq Freeze not implemented 1b=Tx Input Eq Freeze implemented	
	3	Adaptive Tx Input Eq implemented	0b=Adaptive Tx Input Eq not implemented 1b=Adaptive Tx Input Eq implemented	
	2	Tx Input Eq fixed manual control implemented	0b=Tx Input Eq Fixed Manual control not implemented 1b=Tx Input Eq Fixed Manual control implemented	
	1	Tx CDR Bypass control implemented	0b=Tx CDR Bypass control not implemented (if CDR is implemented, it will be enabled) 1b=Tx CDR Bypass control implemented	
	0	Tx CDR implemented	0b=Tx CDR not implemented 1b=Tx CDR implemented	
162	7-6	Reserved		RO RQD
	5	Staged Set 1 implemented	Staged Control Set 1 implemented on Pg 10h	RO RQD
	4-3	Rx Output Eq control implemented	00b=Rx Output Eq control not implemented 01b=Rx Output Eq Pre-cursor control implemented 10b=Rx Output Eq Post-cursor control implemented 11b=Rx Output Eq Pre- and Post-cursor control implemented	
	2	Rx Output Amplitude control implemented	0b=Rx Output Amplitude control not implemented 1b=Rx Output Amplitude control implemented	
	1	Rx CDR Bypass control implemented	0b=Rx CDR Bypass control not implemented (if CDR is implemented, it will be enabled) 1b=Rx CDR Bypass control implemented	
	0	Rx CDR implemented	0b=Rx CDR not implemented 1b=Rx CDR implemented	

1.7.4.11 Media Lane Assignment Options Advertising

Each Application includes five bytes of advertising to define the Application, as described in Section 1.5.2. The first four bytes are defined in Table 26 or Table 48, depending on the ApSel code. The fifth byte is defined in Table 47 for all ApSel codes.

Table 47- Media Lane Assignment Advertising (Page 01h)

Byte	Bits	Name	Description	Type
176	7-0	Media Lane Assignment Options, ApSel 0001b	Coded 1 if the Application is allowed to begin on a given media lane. Bits 0-7 correspond to Host Lanes 1-8. In multi-lane Applications each instance of an Application shall use contiguous media lane numbers. If multiple instances of a single Application are allowed each starting point is identified. If multiple instances are advertised, all instance must be supported concurrently. (See section 1.5.2)	RO RQD
177	7-0	Media Lane Assignment Options, ApSel 0010b		
178	7-0	Media Lane Assignment Options, ApSel 0011b		
179	7-0	Media Lane Assignment Options, ApSel 0100b		
180	7-0	Media Lane Assignment Options, ApSel 0101b		
181	7-0	Media Lane Assignment Options, ApSel 0110b		
182	7-0	Media Lane Assignment Options, ApSel 0111b		
183	7-0	Media Lane Assignment Options, ApSel 1000b		
184	7-0	Media Lane Assignment Options, ApSel 1001b		
185	7-0	Media Lane Assignment Options, ApSel 1010b		
186	7-0	Media Lane Assignment Options, ApSel 1011b		
187	7-0	Media Lane Assignment Options, ApSel 1100b		
188	7-0	Media Lane Assignment Options, ApSel 1101b		
189	7-0	Media Lane Assignment Options, ApSel 1110b		
190	7-0	Media Lane Assignment Options, ApSel 1111b		

1.7.4.12 Additional Application Advertising

Table 48 defines additional module Application advertising fields. The first eight Applications are advertised using Table 26. The Media Lane Assignment Options field for each Application is advertised in Table 47. See Section 1.5.2 for Application advertising methodology.

The first unused entry in Table 48 shall have FFh in the Host Electrical Code field to indicate the end of the list of supported Applications. Table 48 provides space for advertisement of up to seven Applications, in addition to the eight advertised in Table 26.

Module Media Interface encodings are specified by module media interface tables in Appendix C. The required Module Type Encoding field in Byte 85 on the lower page indicates which media interface table applies to the module.

Table 48- Additional Application Advertising Fields (Page 01h)

Byte	Bits	ApSel Code	Name	Description	Type
223	7-0	1001b	Host Electrical Interface Code	Code from Appendix C Table 78	RO Opt.
224	7-0		Module Media Interface Code	Code from Appendix C Table 79-Table 83	
225	7-4		Host Lane Count	0000b=lane count defined by Application code 0001b=1 lane 0010b=2 lanes.... 1000b=8 lanes 1001b-1111b=reserved	
	3-0		Media Lane Count		
226	7-0		Host Lane Assignment Options (See Table 47 for Media Lane Assignment Options)	Bits 0-7 form a bit map and correspond to Host Lanes 1-8. A bit is coded 1 if the Application is allowed to begin on the corresponding host lane. Refer to Section 1.5.2 for details.	

227	7-0	1010b	Host Electrical Interface Code	Code from Appendix C Table 78	RO Opt.
228	7-0		Module Media Interface Code	Code from Appendix C Table 79-Table 83	
229	7-4		Host Lane Count	0000b=lane count defined by Application code 0001b=1 lane 0010b=2 lanes.... 1000b=8 lanes 1001b-1111b=reserved	
	3-0		Media Lane Count		
230	7-0		Host Lane Assignment Options (See Table 47 for Media Lane Assignment Options)	Bits 0-7 form a bit map and correspond to Host Lanes 1-8. A bit is coded 1 if the Application is allowed to begin on the corresponding host lane. Refer to Section 1.5.2 for details.	
231	7-0	1011b	Host Electrical Interface Code	Code from Appendix C Table 78	RO Opt.
232	7-0		Module Media Interface Code	Code from Appendix C Table 79-Table 83	
233	7-4		Host Lane Count	0000b=lane count defined by Application code 0001b=1 lane 0010b=2 lanes.... 1000b=8 lanes 1001b-1111b=reserved	
	3-0		Media Lane Count		
234	7-0		Host Lane Assignment Options (See Table 47 for Media Lane Assignment Options)	Bits 0-7 form a bit map and correspond to Host Lanes 1-8. A bit is coded 1 if the Application is allowed to begin on the corresponding host lane. Refer to Section 1.5.2 for details.	
235	7-0	1100b	Host Electrical Interface Code	Code from Appendix C Table 78	RO Opt.
236	7-0		Module Media Interface Code	Code from Appendix C Table 79-Table 83	
237	7-4		Host Lane Count	0000b=lane count defined by Application code 0001b=1 lane 0010b=2 lanes.... 1000b=8 lanes 1001b-1111b=reserved	
	3-0		Media Lane Count		
238	7-0		Host Lane Assignment Options (See Table 47 for Media Lane Assignment Options)	Bits 0-7 form a bit map and correspond to Host Lanes 1-8. A bit is coded 1 if the Application is allowed to begin on the corresponding host lane. Refer to Section 1.5.2 for details.	
239	7-0	1101b	Host Electrical Interface Code	Code from Appendix C Table 78	RO Opt.
240	7-0		Module Media Interface Code	Code from Appendix C Table 79-Table 83	
241	7-4		Host Lane Count	0000b=lane count defined by Application code 0001b=1 lane 0010b=2 lanes.... 1000b=8 lanes 1001b-1111b=reserved	
	3-0		Media Lane Count		

242	7-0		Host Lane Assignment Options (See Table 47 for Media Lane Assignment Options)	Bits 0-7 form a bit map and correspond to Host Lanes 1-8. A bit is coded 1 if the Application is allowed to begin on the corresponding host lane. Refer to Section 1.5.2 for details.	
243	7-0	1110b	Host Electrical Interface Code	Code from Appendix C Table 78	RO Opt.
244	7-0		Module Media Interface Code	Code from Appendix C Table 79-Table 83	
245	7-4		Host Lane Count	0000b=lane count defined by Application code 0001b=1 lane 0010b=2 lanes.... 1000b=8 lanes 1001b-1111b=reserved	
	3-0		Media Lane Count		
246	7-0		Host Lane Assignment Options (See Table 47 for Media Lane Assignment Options)	Bits 0-7 form a bit map and correspond to Host Lanes 1-8. A bit is coded 1 if the Application is allowed to begin on the corresponding host lane. Refer to Section 1.5.2 for details.	
247	7-0	1111b	Host Electrical Interface Code	Code from Appendix C Table 78	RO Opt.
248	7-0		Module Media Interface Code	Code from Appendix C Table 79-Table 83	
249	7-4		Host Lane Count	0000b=lane count defined by Application code 0001b=1 lane 0010b=2 lanes.... 1000b=8 lanes 1001b-1111b=reserved	
	3-0		Media Lane Count		
250	7-0		Host Lane Assignment Options (See Table 47 for Media Lane Assignment Options)	Bits 0-7 form a bit map and correspond to Host Lanes 1-8. A bit is coded 1 if the Application is allowed to begin on the corresponding host lane. Bits 0-7 correspond to Host Lanes 1-8. Refer to Section 1.5.2 for details.	

1.7.4.13 Checksum

The check code is a one byte code that can be used to verify that the read-only static data on Page 01h is valid. The check code shall be the low order 8 bits of the sum of the contents of all the bytes from byte 130 to byte 254, inclusive. Note that the module firmware revision in bytes 128 and 129 is not included in the checksum.

1.7.5 Upper Page 02h

Upper Page 02h contains the module-defined thresholds for module-level and lane-specific monitors. The presence of Upper Page 02h is advertised in bit 7 in Page 00h byte 2. All fields on Upper Page 02h are read-only and static.

Table 49- Upper Page 02 Overview (Page 02h)

Byte	Size (bytes)	Name	Description
128-175	48	Module-level monitor thresholds	
176-199	24	Lane-specific monitor thresholds	
200-229	30	Reserved	

230-254	25	Customizable space	
255	1	Checksum	Covers bytes 128-254

1.7.5.1 Module-Level Monitor Thresholds

The following thresholds are provided by the module to inform the host of the monitor levels where alarms and warnings will be triggered.

Table 50- Module-Level Monitor Thresholds (Page 02h)

Byte	Bit	Name	Description	Type
128	7-0	Temperature monitor high alarm threshold MSB	Thresholds for internally measured temperature monitor: signed 2's complement in 1/256 degree Celsius increments	RO Opt.
129	7-0	Temperature monitor high alarm threshold LSB		
130	7-0	Temperature monitor low alarm threshold MSB		
131	7-0	Temperature monitor low alarm threshold LSB		
132	7-0	Temperature monitor high warning threshold MSB		
133	7-0	Temperature monitor high warning threshold LSB		
134	7-0	Temperature monitor low warning threshold MSB		
135	7-0	Temperature monitor low warning threshold LSB		
136	7-0	Supply 3.3-volt monitor high alarm threshold MSB	Thresholds for internally measured 3.3 volt input supply voltage: in 100 µV increments	RO Opt.
137	7-0	Supply 3.3-volt monitor high alarm threshold LSB		
138	7-0	Supply 3.3-volt monitor low alarm threshold MSB		
139	7-0	Supply 3.3-volt monitor low alarm threshold LSB		
140	7-0	Supply 3.3-volt monitor high warning threshold MSB		
141	7-0	Supply 3.3-volt monitor high warning threshold LSB		
142	7-0	Supply 3.3-volt monitor low warning threshold MSB		
143	7-0	Supply 3.3-volt monitor low warning threshold LSB		
144	7-0	Aux 1 monitor high alarm threshold MSB	Thresholds for TEC Current or Reserved monitor TEC Current: signed 2's complement in 100/32767% increments of maximum TEC current +32767 is max TEC current (100%) – Max Heating -32767 is min TEC current (100%) – Max Cooling	RO Opt.
145	7-0	Aux 1 monitor high alarm threshold LSB		
146	7-0	Aux 1 monitor low alarm threshold MSB		
147	7-0	Aux 1 monitor low alarm threshold LSB		
148	7-0	Aux 1 monitor high warning threshold MSB		
149	7-0	Aux 1 monitor high warning threshold LSB		
150	7-0	Aux 1 monitor low warning threshold MSB		
151	7-0	Aux 1 monitor low warning threshold LSB		
152	7-0	Aux 2 monitor high alarm threshold MSB	Thresholds for TEC Current or Laser Temperature monitor TEC Current: signed 2's complement in 100/32767% increments of maximum TEC	RO Opt.
153	7-0	Aux 2 monitor high alarm threshold LSB		

154	7-0	Aux 2 monitor low alarm threshold MSB	current+32767 is max TEC current (100%) – Max Heating -32767 is min TEC current (100%) – Max Cooling Laser Temperature: signed 2’s complement in 1/256 degree Celsius increments	
155	7-0	Aux 2 monitor low alarm threshold LSB		
156	7-0	Aux 2 monitor high warning threshold MSB		
157	7-0	Aux 2 monitor high warning threshold LSB		
158	7-0	Aux 2 monitor low warning threshold MSB		
159	7-0	Aux 2 monitor low warning threshold LSB		
160	7-0	Aux 3 monitor high alarm threshold MSB	Thresholds for Laser Temperature or additional supply voltage monitor Laser Temperature: signed 2’s complement in 1/256 degree Celsius increments NOTE: Laser Temp can be below 0 if uncooled or in TX Disable. Additional supply voltage monitor: in 100 µV increments	RO Opt.
161	7-0	Aux 3 monitor high alarm threshold LSB		
162	7-0	Aux 3 monitor low alarm threshold MSB		
163	7-0	Aux 3 monitor low alarm threshold LSB		
164	7-0	Aux 3 monitor high warning threshold MSB		
165	7-0	Aux 3 monitor high warning threshold LSB		
166	7-0	Aux 3 monitor low warning threshold MSB		
167	7-0	Aux 3 monitor low warning threshold LSB		
168	7-0	Custom monitor high alarm threshold MSB	Custom monitor: signed or unsigned 16 bit value	RO Opt.
169	7-0	Custom monitor high alarm threshold LSB		
170	7-0	Custom monitor low alarm threshold MSB		
171	7-0	Custom monitor low alarm threshold LSB		
172	7-0	Custom monitor high warning threshold MSB		
173	7-0	Custom monitor high warning threshold LSB		
174	7-0	Custom monitor low warning threshold MSB		
175	7-0	Custom monitor low warning threshold LSB		

1.7.5.2 Lane-specific Monitor Thresholds

The following thresholds are provided by the module to inform the host of the monitor levels where alarms and warnings will be triggered.

Table 51- Lane-specific Monitor Thresholds (Page 02h, active modules only)

Byte	Bit	Name	Description	Type
176	7-0	Tx optical power monitor high alarm threshold MSB	Threshold for Tx optical power monitor: unsigned integer in 0.1 uW increments, yielding a total measurement range of 0 to 6.5535 mW (~-40 to +8.2 dBm) See section 1.7.7.3 for monitor details including accuracy	RO Opt.
177	7-0	Tx optical power high alarm threshold LSB		
178	7-0	Tx optical power low alarm threshold MSB		
179	7-0	Tx optical power low alarm threshold LSB		
180	7-0	Tx optical power high warning threshold MSB		
181	7-0	Tx optical power high warning threshold LSB		
182	7-0	Tx optical power low warning threshold MSB		
183	7-0	Tx optical power low warning threshold LSB		
184	7-0	Tx bias current monitor high alarm threshold MSB	Threshold for Tx bias monitor: unsigned integer in 2 uA increments, times the multiplier from Table 45. See section 1.7.7.3 for monitor details including accuracy	RO Opt.
185	7-0	Tx bias current high alarm threshold LSB		
186	7-0	Tx bias current low alarm threshold MSB		
187	7-0	Tx bias current low alarm threshold LSB		
188	7-0	Tx bias current high warning threshold MSB		
189	7-0	Tx bias current high warning threshold LSB		
190	7-0	Tx bias current low warning threshold MSB		
191	7-0	Tx bias current low warning threshold LSB		
192	7-0	Rx optical power monitor high alarm threshold MSB	Threshold for Rx optical power monitor: unsigned integer in 0.1 uW increments, yielding a total measurement range of 0 to 6.5535 mW (~-40 to +8.2 dBm) See section 1.7.7.3 for accuracy.	RO Opt.
193	7-0	Rx optical power high alarm threshold LSB		
194	7-0	Rx optical power low alarm threshold MSB		
195	7-0	Rx optical power low alarm threshold LSB		
196	7-0	Rx optical power high warning threshold MSB		
197	7-0	Rx optical power high warning threshold LSB		
198	7-0	Rx optical power low warning threshold MSB		
199	7-0	Rx optical power low warning threshold LSB		

1.7.5.3 Checksum

The check code is a one-byte code that can be used to verify that the device property information in the module is valid. The check code shall be the low order 8 bits of the sum of the contents of all the bytes from byte 128 to byte 254, inclusive.

1.7.6 Upper Page 10h

The upper memory map page 10h is a banked page that contains lane dynamic control bytes. The presence of Upper Page 10h is advertised in bit 7 in Page 00h byte 2. Upper page 10h is subdivided into several areas as illustrated in the following table:

Table 52- Upper Page 16 Overview (Page 10h)

Byte	Size (bytes)	Name	Description
128	1	Data Path Power control	DataPathPwrUp bits for each lane, controls Data Path State machine
129-142	14	Lane-Specific Control	Fields to control lane attributes independent of the Data Path State machine or control sets
143-177	35	Staged Control Set 0	Fields to configure the selected Application Code and signal integrity settings
178-212	35	Staged Control Set 1	Fields to configure the selected Application Code and signal integrity settings
213-231	19	Lane-Specific Flag Masks	
232-239	8	Reserved	
240-255	16	Custom	

1.7.6.1 Data Path Power Control

The DataPathPwrUp byte controls the power and initialization of individual data paths through the Data Path State Machine. The host may set these bits to power up a data path or clear these bits to power down a data path. When one or more DataPathPwrUp bit is set, the corresponding Data Path State Machine shall enter DataPathInit. When one or more DataPathPwrUp bit is cleared, the corresponding Data Path State Machine shall enter DataPathDeinit. Refer to Section 1.5.3 for details about the Data Path State Machine.

Each bit represents a lane. Many data paths consist of multiple lanes. The host shall ensure that all lanes in a data path shall have a consistent state for the DataPathPwrUp bit. When a multi-lane data path is powered up or down, the bits corresponding to all lanes in the data path shall be changed with one two-wire serial transaction. Multiple data paths may be powered up or down at the same time.

The number of lanes in a data path is defined by the selected Application Code in the Active Set (see Table 73). Refer to Section 1.5.2 for details on Application Codes and Section 1.5.4 for details on Control Sets.

Table 53- Data Path Power control (Page 10h, active modules only)

Byte	Bit	Name	Description	Type
128	7	DataPathPwrUp Lane 8	Data Path power control for lane 8 1b=Power Up	RW RQD
	6	DataPathPwrUp Lane 7	Data Path power control for lane 7 1b=Power Up	
	5	DataPathPwrUp Lane 6	Data Path power control for lane 6 1b=Power Up	
	4	DataPathPwrUp Lane 5	Data Path power control for lane 5 1b=Power Up	
	3	DataPathPwrUp Lane 4	Data Path power control for lane 4 1b=Power Up	
	2	DataPathPwrUp Lane 3	Data Path power control for lane 3 1b=Power Up	
	1	DataPathPwrUp Lane 2	Data Path power control for lane 2 1b=Power Up	
	0	DataPathPwrUp Lane 1	Data Path power control for lane 1 1b=Power Up	

1.7.6.2 Lane-Specific Direct Effect Control Fields

The following fields are provided to control certain properties of individual lanes in the module, independent of the data path. In some cases, behaviors may be overridden by data path characteristics (e.g. Tx Disable in DataPathInit). These settings are not staged and have no relationship to Control Sets.

When a Tx output is disabled, it shall have negligible optical output power (Average power <-20dBm). When a Tx output is squelched and not disabled, either the OMA or the Average power (Pave) is reduced on the optical output (See Table 43 and Table 23). In cases where both output Disable and Squelch are applied to the same channel, output Disable shall take precedence. If both Disable TX Squelch and Force TX Squelch are set for one or more channels, the module shall squelch the channel.

Table 54- Lane-specific Control Fields (Page 10h, active modules only)

Byte	Bits	Name	Description	Type
129	7	Tx8 Polarity Flip	0b=No polarity flip for lane 8 1b=Tx input polarity flip for lane 8	RW Opt.
	6	Tx7 Polarity Flip	0b=No polarity flip for lane 7 1b=Tx input polarity flip for lane 7	
	5	Tx6 Polarity Flip	0b=No polarity flip for lane 6 1b=Tx input polarity flip for lane 6	
	4	Tx5 Polarity Flip	0b=No polarity flip for lane 5 1b=Tx input polarity flip for lane 5	
	3	Tx4 Polarity Flip	0b=No polarity flip for lane 4 1b=Tx input polarity flip for lane 4	
	2	Tx3 Polarity Flip	0b=No polarity flip for lane 3 1b=Tx input polarity flip for lane 3	
	1	Tx2 Polarity Flip	0b=No polarity flip for lane 2 1b=Tx input polarity flip for lane 2	
	0	Tx1 Polarity Flip	0b=No polarity flip for lane 1 1b=Tx input polarity flip for lane 1	
130	7	Tx8 Disable	0b=Tx output enabled for media lane 8 1b=Tx output disabled for media lane 8	RW Opt.
	6	Tx7 Disable	0b=Tx output enabled for media lane 7 1b=Tx output disabled for media lane 7	
	5	Tx6 Disable	0b=Tx output enabled for media lane 6 1b=Tx output disabled for media lane 6	

	4	Tx5 Disable	0b=Tx output enabled for media lane 5 1b=Tx output disabled for media lane 5	
	3	Tx4 Disable	0b=Tx output enabled for media lane 4 1b=Tx output disabled for media lane 4	
	2	Tx3 Disable	0b=Tx output enabled for media lane 3 1b=Tx output disabled for media lane 3	
	1	Tx2 Disable	0b=Tx output enabled for media lane 2 1b=Tx output disabled for media lane 2	
	0	Tx1 Disable	0b=Tx output enabled for media lane 1 1b=Tx output disabled for media lane 1	
131	7	Tx8 Squelch Disable	0b=Tx output squelch permitted for media lane 8 1b=Tx output squelch not permitted for media lane 8	RW Opt.
	6	Tx7 Squelch Disable	0b=Tx output squelch permitted for media lane 7 1b=Tx output squelch not permitted for media lane 7	
	5	Tx6 Squelch Disable	0b=Tx output squelch permitted for media lane 6 1b=Tx output squelch not permitted for media lane 6	
	4	Tx5 Squelch Disable	0b=Tx output squelch permitted for media lane 5 1b=Tx output squelch not permitted for media lane 5	
	3	Tx4 Squelch Disable	0b=Tx output squelch permitted for media lane 4 1b=Tx output squelch not permitted for media lane 4	
	2	Tx3 Squelch Disable	0b=Tx output squelch permitted for media lane 3 1b=Tx output squelch not permitted for media lane 3	
	1	Tx2 Squelch Disable	0b=Tx output squelch permitted for media lane 2 1b=Tx output squelch not permitted for media lane 2	
	0	Tx1 Squelch Disable	0b=Tx output squelch permitted for media lane 1 1b=Tx output squelch not permitted for media lane 1	
132	7	Tx8 Force Squelch	0b=No impact on Tx behavior for media lane 8 1b=Tx output squelched for media lane 8	RW Opt.
	6	Tx7 Force Squelch	0b=No impact on Tx behavior for media lane 7 1b=Tx output squelched for media lane 7	
	5	Tx6 Force Squelch	0b=No impact on Tx behavior for media lane 6 1b=Tx output squelched for media lane 6	
	4	Tx5 Force Squelch	0b=No impact on Tx behavior for media lane 5 1b=Tx output squelched for media lane 5	
	3	Tx4 Force Squelch	0b=No impact on Tx behavior for media lane 4 1b=Tx output squelched for media lane 4	
	2	Tx3 Force Squelch	0b=No impact on Tx behavior for media lane 3 1b=Tx output squelched for media lane 3	
	1	Tx2 Force Squelch	0b=No impact on Tx behavior for media lane 2 1b=Tx output squelched for media lane 2	
	0	Tx1 Force Squelch	0b=No impact on Tx behavior for media lane 1 1b=Tx output squelched for media lane 1	
133	7:0	Reserved		RO
134	7	Tx8 Input Eq Adaptation Freeze	0b=Tx input eq adaptation active for lane 8 1b=Tx input eq adaptation frozen at last value for lane 8	RW Opt.
	6	Tx7 Input Eq Adaptation Freeze	0b=Tx input eq adaptation active for lane 7 1b=Tx input eq adaptation frozen at last value for lane 7	

	5	Tx6 Input Eq Adaptation Freeze	0b=Tx input eq adaptation active for lane 6 1b=Tx input eq adaptation frozen at last value for lane 6	
	4	Tx5 Input Eq Adaptation Freeze	0b=Tx input eq adaptation active for lane 5 1b=Tx input eq adaptation frozen at last value for lane 5	
	3	Tx4 Input Eq Adaptation Freeze	0b=Tx input eq adaptation active for lane 4 1b=Tx input eq adaptation frozen at last value for lane 4	
	2	Tx3 Input Eq Adaptation Freeze	0b=Tx input eq adaptation active for lane 3 1b=Tx input eq adaptation frozen at last value for lane 3	
	1	Tx2 Input Eq Adaptation Freeze	0b=Tx input eq adaptation active for lane 2 1b=Tx input eq adaptation frozen at last value for lane 2	
	0	Tx1 Input Eq Adaptation Freeze	0b=Tx input eq adaptation active for lane 1 1b=Tx input eq adaptation frozen at last value for lane 1	
135	7-6	Tx4 Input Eq Adaptation Store	Tx Input Eq Adaptation Store location 00b=reserved 01b=store location 1 10b=store location 2 11b=reserved See section 1.5.5.1	WO Opt.
	5-4	Tx3 Input Eq Adaptation Store		
	3-2	Tx2 Input Eq Adaptation Store		
	1-0	Tx1 Input Eq Adaptation Store		
136	7-6	Tx8 Input Eq Adaptation Store	Tx Input Eq Adaptation Store location 00b=reserved 01b=store location 1 10b=store location 2 11b=reserved See section 1.5.5.1	WO Opt.
	5-4	Tx7 Input Eq Adaptation Store		
	3-2	Tx6 Input Eq Adaptation Store		
	1-0	Tx5 Input Eq Adaptation Store		
137	7	Rx8 Polarity Flip	Ob=No polarity flip for lane 8 1b=Rx output polarity flip for lane 8	RW Opt.
	6	Rx7 Polarity Flip	Ob=No polarity flip for lane 7 1b=Rx output polarity flip for lane 7	
	5	Rx6 Polarity Flip	Ob=No polarity flip for lane 6 1b=Rx output polarity flip for lane 6	
	4	Rx5 Polarity Flip	Ob=No polarity flip for lane 5 1b=Rx output polarity flip for lane 5	
	3	Rx4 Polarity Flip	Ob=No polarity flip for lane 4 1b=Rx output polarity flip for lane 4	
	2	Rx3 Polarity Flip	Ob=No polarity flip for lane 3 1b=Rx output polarity flip for lane 3	
	1	Rx2 Polarity Flip	Ob=No polarity flip for lane 2 1b=Rx output polarity flip for lane 2	
	0	Rx1 Polarity Flip	Ob=No polarity flip for lane 1 1b=Rx output polarity flip for lane 1	
138	7	Rx8 Output Disable	0b=Rx output enabled for lane 8 1b=Rx output disabled for lane 8	RW Opt.
	6	Rx7 Output Disable	0b=Rx output enabled for lane 7 1b=Rx output disabled for lane 7	
	5	Rx6 Output Disable	0b=Rx output enabled for lane 6 1b=Rx output disabled for lane 6	
	4	Rx5 Output Disable	0b=Rx output enabled for lane 5 1b=Rx output disabled for lane 5	

	3	Rx4 Output Disable	0b=Rx output enabled for lane 4 1b=Rx output disabled for lane 4	
	2	Rx3 Output Disable	0b=Rx output enabled for lane 3 1b=Rx output disabled for lane 3	
	1	Rx2 Output Disable	0b=Rx output enabled for lane 2 1b=Rx output disabled for lane 2	
	0	Rx1 Output Disable	0b=Rx output enabled for lane 1 1b=Rx output disabled for lane 1	
139	7	Rx8 Squelch Disable	0b=Rx output squelch permitted for lane 8 1b=Rx output squelch not permitted for lane 8	RW Opt.
	6	Rx7 Squelch Disable	0b=Rx output squelch permitted for lane 7 1b=Rx output squelch not permitted for lane 7	
	5	Rx6 Squelch Disable	0b=Rx output squelch permitted for lane 6 1b=Rx output squelch not permitted for lane 6	
	4	Rx5 Squelch Disable	0b=Rx output squelch permitted for lane 5 1b=Rx output squelch not permitted for lane 5	
	3	Rx4 Squelch Disable	0b=Rx output squelch permitted for lane 4 1b=Rx output squelch not permitted for lane 4	
	2	Rx3 Squelch Disable	0b=Rx output squelch permitted for lane 3 1b=Rx output squelch not permitted for lane 3	
	1	Rx2 Squelch Disable	0b=Rx output squelch permitted for lane 2 1b=Rx output squelch not permitted for lane 2	
	0	Rx1 Squelch Disable	0b=Rx output squelch permitted for lane 1 1b=Rx output squelch not permitted for lane 1	
140-142	All	Reserved		RO

1.7.6.3 Staged Control Set 0

Staged Control Set 0 is required for all modules. Refer to Section 1.5.4 for background on Control Set methodology. The host should write the Apply_DataPathInit and Apply_Immediate bytes with one-byte writes.

Table 55- Staged Control Set 0, Apply Controls (Page 10h, active modules only)

Byte	Bits	Name	Description	Type
143	7	Staged Set 0 Lane 8 Apply_DataPathInit	Apply Staged Control Set 0 lane 8 settings using DataPathInit 1b=Apply Stage Control Set	WO RQD
	6	Staged Set 0 Lane 7 Apply_DataPathInit	Apply Staged Control Set 0 lane 7 settings using DataPathInit 1b=Apply Stage Control Set	
	5	Staged Set 0 Lane 6 Apply_DataPathInit	Apply Staged Control Set 0 lane 6 settings using DataPathInit 1b=Apply Stage Control Set	
	4	Staged Set 0 Lane 5 Apply_DataPathInit	Apply Staged Control Set 0 lane 5 settings using DataPathInit 1b=Apply Stage Control Set	
	3	Staged Set 0 Lane 4 Apply_DataPathInit	Apply Staged Control Set 0 lane 4 settings using DataPathInit 1b=Apply Stage Control Set	
	2	Staged Set 0 Lane 3 Apply_DataPathInit	Apply Staged Control Set 0 lane 3 settings using DataPathInit 1b=Apply Stage Control Set	
	1	Staged Set 0 Lane 2 Apply_DataPathInit	Apply Staged Control Set 0 lane 2 settings using DataPathInit 1b=Apply Stage Control Set	

	0	Staged Set 0 Lane 1 Apply_DataPathInit	Apply Staged Control Set 0 lane 1 settings using DataPathInit 1b=Apply Stage Control Set	
144	7	Staged Set 0 Lane 8 Apply_Immediate	Apply Staged Control Set 0 lane 8 settings with no Data Path State transitions 1b=Apply Stage Control Set	WO RQD
	6	Staged Set 0 Lane 7 Apply_Immediate	Apply Staged Control Set 0 lane 7 settings with no Data Path State transitions 1b=Apply Stage Control Set	
	5	Staged Set 0 Lane 6 Apply_Immediate	Apply Staged Control Set 0 lane 6 settings with no Data Path State transitions 1b=Apply Stage Control Set	
	4	Staged Set 0 Lane 5 Apply_Immediate	Apply Staged Control Set 0 lane 5 settings with no Data Path State transitions 1b=Apply Stage Control Set	
	3	Staged Set 0 Lane 4 Apply_Immediate	Apply Staged Control Set 0 lane 4 settings with no Data Path State transitions 1b=Apply Stage Control Set	
	2	Staged Set 0 Lane 3 Apply_Immediate	Apply Staged Control Set 0 lane 3 settings with no Data Path State transitions 1b=Apply Stage Control Set	
	1	Staged Set 0 Lane 2 Apply_Immediate	Apply Staged Control Set 0 lane 2 settings with no Data Path State transitions 1b=Apply Stage Control Set	
	0	Staged Set 0 Lane 1 Apply_Immediate	Apply Staged Control Set 0 lane 1 settings with no Data Path State transitions 1b=Apply Stage Control Set	

The following fields allow the host to select one or more of the Applications supported and advertised by the module in Table 26 and Table 48. A set of fields is provided for each lane, however Applications that span multiple lanes shall have the same ApSel code and Data Path code for all lanes in the data path. Changes to these fields are not applied until the corresponding lane bits in Apply_DataPathInit or Apply_Immediate are set.

The ApSel Codes shall be one of the module-advertised Application Codes from Table 26 or Table 48. The Data Path code identifies the first lane in the data path. For example, a data path including lane 1 would be coded 000b and a data path where lane 5 is the lower lane number would be coded 100b. Explicit Control (bit 0 in bytes 145-152) allows the host to specify signal integrity settings rather than use the Application defined settings. These settings may be specified using Table 57 and Table 58.

Table 56- Staged Control Set 0, Application Select Controls (Page 10h, active modules only)

Byte	Bits	Name	Description	Type
145	7-4	Staged Set 0 Lane 1 Application code	ApSel code from Table 26 or Table 48, lane 1	RW RQD
	3-1	Staged Set 0 Lane 1 Data Path code	First lane in the data path containing lane 1 000b=Lane 1	
	0	Staged Set 0 Lane 1 Explicit Control	0b=Use Application-defined settings for lane 1 1b=use Staged Set 0 control values for lane 1	
146	7-4	Staged Set 0 Lane 2 Application code	ApSel code from Table 26 or Table 48, lane 2	RW RQD
	3-1	Staged Set 0 Lane 2 Data Path code	First lane in the data path containing lane 2 000b=Lane 1, 001b=Lane 2	
	0	Staged Set 0 Lane 2 Explicit Control	0b=Use Application-defined settings for lane 2 1b=use Staged Set 0 control values for lane 2	
147	7-4	Staged Set 0 Lane 3 Application code	ApSel code from Table 26 or Table 48, lane 3	RW RQD

	3-1	Staged Set 0 Lane 3 Data Path code	First lane in the data path containing lane 3 000b=Lane 1, 001b=Lane 2, etc.	
	0	Staged Set 0 Lane 3 Explicit Control	0b=Use Application-defined settings for lane 3 1b=use Staged Set 0 control values for lane 3	
148	7-4	Staged Set 0 Lane 4 Application code	ApSel code from Table 26 or Table 48, lane 4	RW RQD
	3-1	Staged Set 0 Lane 4 Data Path code	First lane in the data path containing lane 4 000b=Lane 1, 001b=Lane 2, etc.	
	0	Staged Set 0 Lane 4 Explicit Control	0b=Use Application-defined settings for lane 4 1b=use Staged Set 0 control values for lane 4	
149	7-4	Staged Set 0 Lane 5 Application code	ApSel code from Table 26 or Table 48, lane 5	RW RQD
	3-1	Staged Set 0 Lane 5 Data Path code	First lane in the data path containing lane 5 000b=Lane 1, 001b=Lane 2, etc.	
	0	Staged Set 0 Lane 5 Explicit Control	0b=Use Application-defined settings for lane 5 1b=use Staged Set 0 control values for lane 5	
150	7-4	Staged Set 0 Lane 6 Application code	ApSel code from Table 26 or Table 48, lane 6	RW RQD
	3-1	Staged Set 0 Lane 6 Data Path code	First lane in the data path containing lane 6 000b=Lane 1, 001b=Lane 2, etc.	
	0	Staged Set 0 Lane 6 Explicit Control	0b=Use Application-defined settings for lane 6 1b=use Staged Set 0 control values for lane 6	
151	7-4	Staged Set 0 Lane 7 Application code	ApSel code from Table 26 or Table 48, lane 7	RW RQD
	3-1	Staged Set 0 Lane 7 Data Path code	First lane in the data path containing lane 7 000b=Lane 1, 001b=Lane 2, etc.	
	0	Staged Set 0 Lane 7 Explicit Control	0b=Use Application-defined settings for lane 7 1b=use Staged Set 0 control values for lane 7	
152	7-4	Staged Set 0 Lane 8 Application code	ApSel code from Table 26 or Table 48, lane 8	RW RQD
	3-1	Staged Set 0 Lane 8 Data Path code	First lane in the data path containing lane 8 000b=Lane 1, 001b=Lane 2, etc.	
	0	Staged Set 0 Lane 8 Explicit Control	0b=Use Application default settings for lane 8 1b=use Staged Set 0 control values for lane 8	

The following fields allow the host to specify the signal integrity settings for a lane rather than use the defaults associated with the selected Application Code. See Table 10 for the dependency of these fields on the value of the Explicit Control bit. Changes to these fields are not applied until the corresponding lane bits in Apply_DataPathInit or Apply_Immediate are set. See section 1.5.5 for definitions of valid signal integrity control settings.

Table 57- Staged Control Set 0, Tx Controls (Page 10h, active modules only)

Byte	Bits	Name	Description	Type
153	7	Staged Set 0 Tx8 Adaptive Input Eq Enable	1b=Enable 0b=Disable (use manual fixed EQ)	RW Opt.
	6	Staged Set 0 Tx7 Adaptive Input Eq Enable	1b=Enable 0b=Disable (use manual fixed EQ)	
	5	Staged Set 0 Tx6 Adaptive Input Eq Enable	1b=Enable 0b=Disable (use manual fixed EQ)	
	4	Staged Set 0 Tx5 Adaptive Input Eq Enable	1b=Enable 0b=Disable (use manual fixed EQ)	
	3	Staged Set 0 Tx4 Adaptive Input Eq Enable	1b=Enable 0b=Disable (use manual fixed EQ)	
	2	Staged Set 0 Tx3 Adaptive Input Eq Enable	1b=Enable 0b=Disable (use manual fixed EQ)	
	1	Staged Set 0 Tx2 Adaptive Input Eq Enable	1b=Enable 0b=Disable (use manual fixed EQ)	

	0	Staged Set 0 Tx1 Adaptive Input Eq Enable	1b=Enable 0b=Disable (use manual fixed EQ)	
154	7-6	Staged Set 0 Tx4 Adaptive Input Eq Recall	Recall stored Tx Eq adaptation value, 00b=do not Recall 01b=store location 1 10b=store location 2 11b=reserved See section 1.5.5.1 for Store/Recall methodology	RW Opt.
	5-4	Staged Set 0 Tx3 Adaptive Input Eq Recall		
	3-2	Staged Set 0 Tx2 Adaptive Input Eq Recall		
	1-0	Staged Set 0 Tx1 Adaptive Input Eq Recall		
155	7-6	Staged Set 0 Tx8 Adaptive Input Eq Recall	Recall stored Tx Eq adaptation value, 00b=do not Recall 01b=store location 1 10b=store location 2 11b=reserved See section 1.5.5.1 for Store/Recall methodology	RW Opt.
	5-4	Staged Set 0 Tx7 Adaptive Input Eq Recall		
	3-2	Staged Set 0 Tx6 Adaptive Input Eq Recall		
	1-0	Staged Set 0 Tx5 Adaptive Input Eq Recall		
156	7-4	Staged Set 0 Tx2 Input Eq control	Manual fixed Tx input eq control (See Table 10)	RW Opt.
	3-0	Staged Set 0 Tx1 Input Eq control	Manual fixed Tx input eq control (See Table 10)	
157	7-4	Staged Set 0 Tx4 Input Eq control	Manual fixed Tx input eq control (See Table 10)	RW Opt.
	3-0	Staged Set 0 Tx3 Input Eq control	Manual fixed Tx input eq control (See Table 10)	
158	7-4	Staged Set 0 Tx6 Input Eq control	Manual fixed Tx input eq control (See Table 10)	RW Opt.
	3-0	Staged Set 0 Tx5 Input Eq control	Manual fixed Tx input eq control (See Table 10)	
159	7-4	Staged Set 0 Tx8 Input Eq control	Manual fixed Tx input eq control (See Table 10)	RW Opt.
	3-0	Staged Set 0 Tx7 Input Eq control	Manual fixed Tx input eq control (See Table 10)	
160	7	Staged Set 0 Tx8 CDR control	1b=CDR enabled, 0b=CDR bypassed	RW Opt.
	6	Staged Set 0 Tx7 CDR control	1b=CDR enabled, 0b=CDR bypassed	
	5	Staged Set 0 Tx6 CDR control	1b=CDR enabled, 0b=CDR bypassed	
	4	Staged Set 0 Tx5 CDR control	1b=CDR enabled, 0b=CDR bypassed	
	3	Staged Set 0 Tx4 CDR control	1b=CDR enabled, 0b=CDR bypassed	
	2	Staged Set 0 Tx3 CDR control	1b=CDR enabled, 0b=CDR bypassed	
	1	Staged Set 0 Tx2 CDR control	1b=CDR enabled, 0b=CDR bypassed	
	0	Staged Set 0 Tx1 CDR control	1b=CDR enabled, 0b=CDR bypassed	

Table 58- Staged Control Set 0, Rx Controls (Page 10h, active modules only)

Byte	Bits	Name	Description	Type
161	7	Staged Set 0 Rx8 CDR control	1b=CDR enabled, 0b=CDR bypassed	RW Opt.
	6	Staged Set 0 Rx7 CDR control	1b=CDR enabled, 0b=CDR bypassed	

	5	Staged Set 0 Rx6 CDR control	1b=CDR enabled, 0b=CDR bypassed	
	4	Staged Set 0 Rx5 CDR control	1b=CDR enabled, 0b=CDR bypassed	
	3	Staged Set 0 Rx4 CDR control	1b=CDR enabled, 0b=CDR bypassed	
	2	Staged Set 0 Rx3 CDR control	1b=CDR enabled, 0b=CDR bypassed	
	1	Staged Set 0 Rx2 CDR control	1b=CDR enabled, 0b=CDR bypassed	
	0	Staged Set 0 Rx1 CDR control	1b=CDR enabled, 0b=CDR bypassed	
162	7-4	Staged Set 0 Rx2 Output Eq control, pre-cursor	Rx output equalization pre-cursor (See Table 13)	RW Opt.
	3-0	Staged Set 0 Rx1 Output Eq control, pre-cursor	Rx output equalization pre-cursor (See Table 13)	
163	7-4	Staged Set 0 Rx4 Output Eq control, pre-cursor	Rx output equalization pre-cursor (See Table 13)	RW Opt.
	3-0	Staged Set 0 Rx3 Output Eq control, pre-cursor	Rx output equalization pre-cursor (See Table 13)	
164	7-4	Staged Set 0 Rx6 Output Eq control, pre-cursor	Rx output equalization pre-cursor (See Table 13)	RW Opt.
	3-0	Staged Set 0 Rx5 Output Eq control, pre-cursor	Rx output equalization pre-cursor (See Table 13)	
165	7-4	Staged Set 0 Rx8 Output Eq control, pre-cursor	Rx output equalization pre-cursor (See Table 13)	RW Opt.
	3-0	Staged Set 0 Rx7 Output Eq control, pre-cursor	Rx output equalization pre-cursor (See Table 13)	
166	7-4	Staged Set 0 Rx2 Output Eq control, post-cursor	Rx output equalization post-cursor (See Table 13)	RW Opt.
	3-0	Staged Set 0 Rx1 Output Eq control, post-cursor	Rx output equalization post-cursor (See Table 13)	
167	7-4	Staged Set 0 Rx4 Output Eq control, post-cursor	Rx output equalization post-cursor (See Table 13)	RW Opt.
	3-0	Staged Set 0 Rx3 Output Eq control, post-cursor	Rx output equalization post-cursor (See Table 13)	
168	7-4	Staged Set 0 Rx6 Output Eq control, post-cursor	Rx output equalization post-cursor (See Table 13)	RW Opt.
	3-0	Staged Set 0 Rx5 Output Eq control, post-cursor	Rx output equalization post-cursor (See Table 13)	
169	7-4	Staged Set 0 Rx8 Output Eq control, post-cursor	Rx output equalization post-cursor (See Table 13)	RW Opt.
	3-0	Staged Set 0 Rx7 Output Eq control, post-cursor	Rx output equalization post-cursor (See Table 13)	
170	7-4	Staged Set 0 Rx2 Output Amplitude control	Rx output amplitude (see Table 14)	RW Opt.
	3-0	Staged Set 0 Rx1 Output Amplitude control	Rx output amplitude (see Table 14)	
171	7-4	Staged Set 0 Rx4 Output Amplitude control	Rx output amplitude (see Table 14)	RW Opt.
	3-0	Staged Set 0 Rx3 Output Amplitude control	Rx output amplitude (see Table 14)	
172	7-4	Staged Set 0 Rx6 Output Amplitude control	Rx output amplitude (see Table 14)	RW Opt.
	3-0	Staged Set 0 Rx5 Output Amplitude control	Rx output amplitude (see Table 14)	
173	7-4	Staged Set 0 Rx8 Output Amplitude control	Rx output amplitude (see Table 14)	RW Opt.

	3-0	Staged Set 0 Rx7 Output Amplitude control	Rx output amplitude (see Table 14)	
174-177	All	Reserved		RO

1.7.6.4 Staged Control Set 1

Staged Control Set 1 is MSA optional for all modules but may be needed for some Applications where speed negotiation is performed. The module advertises support for Staged Control Set 1 in Table 40. Refer to Section 1.5.4 for background on Control Set methodology. The host should write the Apply_DataPathInit and Apply_Immediate bytes with one-byte writes.

Table 59- Staged Control Set 1, Apply Controls (Page 10h, active modules only)

Byte	Bits	Name	Description	Type
178	7	Staged Set 1 Lane 8 Apply_DataPathInit	Apply Staged Control Set 1 lane 8 settings using DataPathInit 1b=Apply Stage Control Set	WO Opt.
	6	Staged Set 1 Lane 7 Apply_DataPathInit	Apply Staged Control Set 1 lane 7 settings using DataPathInit 1b=Apply Stage Control Set	
	5	Staged Set 1 Lane 6 Apply_DataPathInit	Apply Staged Control Set 1 lane 6 settings using DataPathInit 1b=Apply Stage Control Set	
	4	Staged Set 1 Lane 5 Apply_DataPathInit	Apply Staged Control Set 1 lane 5 settings using DataPathInit 1b=Apply Stage Control Set	
	3	Staged Set 1 Lane 4 Apply_DataPathInit	Apply Staged Control Set 1 lane 4 settings using DataPathInit 1b=Apply Stage Control Set	
	2	Staged Set 1 Lane 3 Apply_DataPathInit	Apply Staged Control Set 1 lane 3 settings using DataPathInit 1b=Apply Stage Control Set	
	1	Staged Set 1 Lane 2 Apply_DataPathInit	Apply Staged Control Set 1 lane 2 settings using DataPathInit 1b=Apply Stage Control Set	
	0	Staged Set 1 Lane 1 Apply_DataPathInit	Apply Staged Control Set 1 lane 1 settings using DataPathInit 1b=Apply Stage Control Set	
179	7	Staged Set 1 Lane 8 Apply_Immediate	Apply Staged Control Set 1 lane 8 settings with no Data Path State transitions 1b=Apply Stage Control Set	WO Opt.
	6	Staged Set 1 Lane 7 Apply_Immediate	Apply Staged Control Set 1 lane 7 settings with no Data Path State transitions 1b=Apply Stage Control Set	
	5	Staged Set 1 Ln6 Apply_Immediate	Apply Staged Control Set 1 lane 6 settings with no Data Path State transitions 1b=Apply Stage Control Set	
	4	Staged Set 1 Lane 5 Apply_Immediate	Apply Staged Control Set 1 lane 5 settings with no Data Path State transitions 1b=Apply Stage Control Set	
	3	Staged Set 1 Lane 4 Apply_Immediate	Apply Staged Control Set 1 lane 4 settings with no Data Path State transitions 1b=Apply Stage Control Set	
	2	Staged Set 1 Lane 3 Apply_Immediate	Apply Staged Control Set 1 lane 3 settings with no Data Path State transitions 1b=Apply Stage Control Set	

	1	Staged Set 1 Lane 2 Apply_Immediate	Apply Staged Control Set 1 lane 2 settings with no Data Path State transitions 1b=Apply Stage Control Set	
	0	Staged Set 1 Lane 1 Apply_Immediate	Apply Staged Control Set 1 lane 1 settings with no Data Path State transitions 1b=Apply Stage Control Set	

The following fields allow the host to select a signaling rate, modulation format, and data path width. A set of fields is provided for each lane, however Applications that span multiple lanes shall have the same Application code and Data Path code for all lanes in the data path. Changes to these fields are not applied until the corresponding lane bits in Apply_DataPathInit or Apply_Immediate are set.

The Application Code shall be one of the module-advertised ApSel Codes from Table 26 or Table 48. The Data Path code identifies the first lane in the data path. For example, a data path including lane 1 would be coded 000b and a data path where lane 5 is the lower lane number would be coded 100b. Explicit Control (bit 0 in bytes 180-187) allows the host to specify signal integrity settings rather than use the Application-defined settings. These settings may be specified using Table 61 and Table 62.

Table 60- Staged Control Set 1, Application Select Controls (Page 10h, active modules only)

Byte	Bits	Name	Description	Type
180	7-4	Staged Set 1 Lane 1 Application code	ApSel code from Table 26 or Table 48, lane 1	RW Opt.
	3-1	Staged Set 1 Lane 1 Data Path code	First lane in the data path containing lane 1 000b=Lane 1	
	0	Staged Set 1 Lane 1 Explicit Control	0b=Use Application-defined settings for lane 1 1b=use Staged Set 1 control values for lane 1	
181	7-4	Staged Set 1 Lane 2 Application code	ApSel code from Table 26 or Table 48, lane 2	RW Opt.
	3-1	Staged Set 1 Lane 2 Data Path code	First lane in the data path containing lane 2 000b=Lane 1, 001b=Lane 2	
	0	Staged Set 1 Lane 2 Explicit Control	0b=Use Application-defined settings for lane 2 1b=use Staged Set 1 control values for lane 2	
182	7-4	Staged Set 1 Lane 3 Application code	ApSel code from Table 26 or Table 48, lane 3	RW Opt.
	3-1	Staged Set 1 Lane 3 Data Path code	First lane in the data path containing lane 3 000b=Lane 1, 001b=Lane 2, etc.	
	0	Staged Set 1 Lane 3 Explicit Control	0b=Use Application-defined settings for lane 3 1b=use Staged Set 1 control values for lane 3	
183	7-4	Staged Set 1 Lane 4 Application code	ApSel code from Table 26 or Table 48, lane 4	RW Opt.
	3-1	Staged Set 1 Lane 4 Data Path code	First lane in the data path containing lane 4 000b=Lane 1, 001b=Lane 2, etc.	
	0	Staged Set 1 Lane 4 Explicit Control	0b=Use Application-defined settings for lane 4 1b=use Staged Set 1 control values for lane 4	
184	7-4	Staged Set 1 Lane 5 Application code	ApSel code from Table 26 or Table 48, lane 5	RW Opt.
	3-1	Staged Set 1 Lane 5 Data Path code	First lane in the data path containing lane 5 000b=Lane 1, 001b=Lane 2, etc.	
	0	Staged Set 1 Lane 5 Explicit Control	0b=Use Application-defined settings for lane 5 1b=use Staged Set 1 control values for lane 5	
185	7-4	Staged Set 1 Lane 6 Application code	ApSel code from Table 26 or Table 48, lane 6	RW Opt.

	3-1	Staged Set 1 Lane 6 Data Path code	First lane in the data path containing lane 6 000b=Lane 1, 001b=Lane 2, etc.	
	0	Staged Set 1 Lane 6 Explicit Control	0b=Use Application-defined settings for lane 6 1b=use Staged Set 1 control values for lane 6	
186	7-4	Staged Set 1 Lane 7 Application code	ApSel code from Table 26 or Table 48, lane 7	RW Opt.
	3-1	Staged Set 1 Lane 7 Data Path code	First lane in the data path containing lane 7 000b=Lane 1, 001b=Lane 2, etc.	
	0	Staged Set 1 Lane 7 Explicit Control	0b=Use Application-defined settings for lane 7 1b=use Staged Set 1 control values for lane 7	
187	7-4	Staged Set 1 Lane 8 Application code	ApSel code from Table 26 or Table 48, lane 8	RW Opt.
	3-1	Staged Set 1 Lane 8 Data Path code	First lane in the data path containing lane 8 000b=Lane 1, 001b=Lane 2, etc.	
	0	Staged Set 1 Lane 8 Explicit Control	0b=Use Application-defined settings for lane 8 1b=use Staged Set 1 control values for lane 8	

The following fields allow the host to specify the signal integrity settings for a lane rather than use the defaults associated with the selected Application Code. See Table 10 for the dependency of these fields on the value of the Explicit Control bit. Changes to these fields are not applied until the corresponding lane bits in Apply_DataPathInit or Apply_Immediate are set. See Section 1.5.5 for definitions of valid signal integrity control settings.

Table 61- Staged Control Set 1, Tx Controls (Page 10h, active modules only)

Byte	Bits	Name	Description	Type
188	7	Staged Set 1 Tx8 Adaptive Input Eq Enable	1b=Enable 0b=Disable (use manual fixed EQ)	RW Opt.
	6	Staged Set 1 Tx7 Adaptive Input Eq Enable	1b=Enable 0b=Disable (use manual fixed EQ)	
	5	Staged Set 1 Tx6 Adaptive Input Eq Enable	1b=Enable 0b=Disable (use manual fixed EQ)	
	4	Staged Set 1 Tx5 Adaptive Input Eq Enable	1b=Enable 0b=Disable (use manual fixed EQ)	
	3	Staged Set 1 Tx4 Adaptive Input Eq Enable	1b=Enable 0b=Disable (use manual fixed EQ)	
	2	Staged Set 1 Tx3 Adaptive Input Eq Enable	1b=Enable 0b=Disable (use manual fixed EQ)	
	1	Staged Set 1 Tx2 Adaptive Input Eq Enable	1b=Enable 0b=Disable (use manual fixed EQ)	
	0	Staged Set 1 Tx1 Adaptive Input Eq Enable	1b=Enable 0b=Disable (use manual fixed EQ)	
189	7-6	Staged Set 1 Tx4 Adaptive Input Eq Recall	Recall stored Tx Eq adaptation value, 00b=do not recall 01b=store location 1 10b=store location 2 11b=reserved See section 1.5.5.1 for Store/Recall methodology	RW Opt.
	5-4	Staged Set 1 Tx3 Adaptive Input Eq Recall		
	3-2	Staged Set 1 Tx2 Adaptive Input Eq Recall		
	1-0	Staged Set 1 Tx1 Adaptive Input Eq Recall		
190	7-6	Staged Set 1 Tx8 Adaptive Input Eq Recall	Recall stored Tx Eq adaptation value, 00b=do not recall 01b=store location 1 10b=store location 2	RW Opt.
	5-4	Staged Set 1 Tx7 Adaptive Input Eq Recall		

	3-2	Staged Set 1 Tx6 Adaptive Input Eq Recall	11b=reserved See section 1.5.5.1 for Store/Recall methodology	
	1-0	Staged Set 1 Tx5 Adaptive Input Eq Recall		
191	7-4	Staged Set 1 Tx2 Input Eq control	Manual fixed Tx input eq control (see Table 12)	RW Opt.
	3-0	Staged Set 1 Tx1 Input Eq control	Manual fixed Tx input eq control (see Table 12)	
192	7-4	Staged Set 1 Tx4 Input Eq control	Manual fixed Tx input eq control (see Table 12)	RW Opt.
	3-0	Staged Set 1 Tx3 Input Eq control	Manual fixed Tx input eq control (see Table 12)	
193	7-4	Staged Set 1 Tx6 Input Eq control	Manual fixed Tx input eq control (see Table 12)	RW Opt.
	3-0	Staged Set 1 Tx5 Input Eq control	Manual fixed Tx input eq control (see Table 12)	
194	7-4	Staged Set 1 Tx8 Input Eq control	Manual fixed Tx input eq control (see Table 12)	RW Opt.
	3-0	Staged Set 1 Tx7 Input Eq control	Manual fixed Tx input eq control (see Table 12)	
195	7	Staged Set 1 Tx8 CDR control	1b=CDR enabled, 0b=CDR bypassed	RW Opt.
	6	Staged Set 1 Tx7 CDR control	1b=CDR enabled, 0b=CDR bypassed	
	5	Staged Set 1 Tx6 CDR control	1b=CDR enabled, 0b=CDR bypassed	
	4	Staged Set 1 Tx5 CDR control	1b=CDR enabled, 0b=CDR bypassed	
	3	Staged Set 1 Tx4 CDR control	1b=CDR enabled, 0b=CDR bypassed	
	2	Staged Set 1 Tx3 CDR control	1b=CDR enabled, 0b=CDR bypassed	
	1	Staged Set 1 Tx2 CDR control	1b=CDR enabled, 0b=CDR bypassed	
	0	Staged Set 1 Tx1 CDR control	1b=CDR enabled, 0b=CDR bypassed	

Table 62- Staged Control Set 1, Rx Controls (Page 10h, active modules only)

Byte	Bits	Name	Description	Type
196	7	Staged Set 1 Rx8 CDR control	1b=CDR enabled, 0b=CDR bypassed	RW Opt.
	6	Staged Set 1 Rx7 CDR control	1b=CDR enabled, 0b=CDR bypassed	
	5	Staged Set 1 Rx6 CDR control	1b=CDR enabled, 0b=CDR bypassed	
	4	Staged Set 1 Rx5 CDR control	1b=CDR enabled, 0b=CDR bypassed	
	3	Staged Set 1 Rx4 CDR control	1b=CDR enabled, 0b=CDR bypassed	
	2	Staged Set 1 Rx3 CDR control	1b=CDR enabled, 0b=CDR bypassed	
	1	Staged Set 1 Rx2 CDR control	1b=CDR enabled, 0b=CDR bypassed	
	0	Staged Set 1 Rx1 CDR control	1b=CDR enabled, 0b=CDR bypassed	
197	7-4	Staged Set 1 Rx2 Output Eq control, pre-cursor	Rx output equalization pre-cursor (See Table 13)	RW Opt.

	3-0	Staged Set 1 Rx1 Output Eq control, pre-cursor	Rx output equalization pre-cursor (See Table 13)	
198	7-4	Staged Set 1 Rx4 Output Eq control, pre-cursor	Rx output equalization pre-cursor (See Table 13)	RW Opt.
	3-0	Staged Set 1 Rx3 Output Eq control, pre-cursor	Rx output equalization pre-cursor (See Table 13)	
199	7-4	Staged Set 1 Rx6 Output Eq control, pre-cursor	Rx output equalization pre-cursor (See Table 13)	RW Opt.
	3-0	Staged Set 1 Rx5 Output Eq control, pre-cursor	Rx output equalization pre-cursor (See Table 13)	
200	7-4	Staged Set 1 Rx8 Output Eq control, pre-cursor	Rx output equalization pre-cursor (See Table 13)	RW Opt.
	3-0	Staged Set 1 Rx7 Output Eq control, pre-cursor	Rx output equalization pre-cursor (See Table 13)	
201	7-4	Staged Set 1 Rx2 Output Eq control, post-cursor	Rx output equalization post-cursor (See Table 13)	RW Opt.
	3-0	Staged Set 1 Rx1 Output Eq control, post-cursor	Rx output equalization post-cursor (See Table 13)	
202	7-4	Staged Set 1 Rx4 Output Eq control, post-cursor	Rx output equalization post-cursor (See Table 13)	RW Opt.
	3-0	Staged Set 1 Rx3 Output Eq control, post-cursor	Rx output equalization post-cursor (See Table 13)	
203	7-4	Staged Set 1 Rx6 Output Eq control, post-cursor	Rx output equalization post-cursor (See Table 13)	RW Opt.
	3-0	Staged Set 1 Rx5 Output Eq control, post-cursor	Rx output equalization post-cursor (See Table 13)	
204	7-4	Staged Set 1 Rx8 Output Eq control, post-cursor	Rx output equalization post-cursor (See Table 13)	RW Opt.
	3-0	Staged Set 1 Rx7 Output Eq control, post-cursor	Rx output equalization post-cursor (See Table 13)	
205	7-4	Staged Set 1 Rx2 Output Amplitude control	Rx output amplitude encoding (see Table 14)	RW Opt.
	3-0	Staged Set 1 Rx1 Output Amplitude control	Rx output amplitude encoding (see Table 14)	
206	7-4	Staged Set 1 Rx4 Output Amplitude control	Rx output amplitude encoding (see Table 14)	RW Opt.
	3-0	Staged Set 1 Rx3 Output Amplitude control	Rx output amplitude encoding (see Table 14)	
207	7-4	Staged Set 1 Rx6 Output Amplitude control	Rx output amplitude encoding (see Table 14)	RW Opt.
	3-0	Staged Set 1 Rx5 Output Amplitude control	Rx output amplitude encoding (see Table 14)	
208	7-4	Staged Set 1 Rx8 Output Amplitude control	Rx output amplitude encoding (see Table 14)	RW Opt.
	3-0	Staged Set 1 Rx7 Output Amplitude control	Rx output amplitude encoding (see Table 14)	
209-212	All	Reserved		RO

1.7.6.5 Lane-Specific Flag Masks

The host may control which flags result in a hardware interrupt by setting masking bits in Table 63. For example, the mask bits may be used to prevent an interrupt request from remaining active while the host performs actions to acknowledge and handle the interrupt condition. A mask bit is allocated for each flag bit.

A value of 1 in a masking bit prevents the assertion of the hardware interrupt signal, if one exists, by the corresponding latched flag bit. Masking bits are volatile: at power up or exit from module reset, all mask bits shall be clear.

Table 63- Lane-Specific Flag Masks (Page 10h, active modules only)

Byte	Bits	Name	Description	Type
213	7	M-Lane 8 Data Path State Changed flag mask	Masking bit for Data Path State Changed flag, lane 8	RW RQD
	6	M-Lane 7 Data Path State Changed flag mask	Masking bit for Data Path State Changed flag, lane 7	
	5	M-Lane 6 Data Path State Changed flag mask	Masking bit for Data Path State Changed flag, lane 6	
	4	M-Lane 5 Data Path State Changed flag mask	Masking bit for Data Path State Changed flag, lane 5	
	3	M-Lane 4 Data Path State Changed flag mask	Masking bit for Data Path State Changed flag, lane 4	
	2	M-Lane 3 Data Path State Changed flag mask	Masking bit for Data Path State Changed flag, lane 3	
	1	M-Lane 2 Data Path State Changed flag mask	Masking bit for Data Path State Changed flag, lane 2	
	0	M-Lane 1 Data Path State Changed flag mask	Masking bit for Data Path State Changed flag, lane 1	
214	7	M-Tx8 Fault flag mask	Masking bit for Tx Fault flag, media lane 8	RW Opt.
	6	M-Tx7 Fault flag mask	Masking bit for Tx Fault flag, media lane 7	
	5	M-Tx6 Fault flag mask	Masking bit for Tx Fault flag, media lane 6	
	4	M-Tx5 Fault flag mask	Masking bit for Tx Fault flag, media lane 5	
	3	M-Tx4 Fault flag mask	Masking bit for Tx Fault flag, media lane 4	
	2	M-Tx3 Fault flag mask	Masking bit for Tx Fault flag, media lane 3	
	1	M-Tx2 Fault flag mask	Masking bit for Tx Fault flag, media lane 2	
	0	M-Tx1 Fault flag mask	Masking bit for Tx Fault flag, media lane 1	
215	7	M-Tx8 LOS flag mask	Masking bit for Tx LOS flag, lane 8	RW Opt.
	6	M-Tx7 LOS flag mask	Masking bit for Tx LOS flag, lane 7	
	5	M-Tx6 LOS flag mask	Masking bit for Tx LOS flag, lane 6	
	4	M-Tx5 LOS flag mask	Masking bit for Tx LOS flag, lane 5	
	3	M-Tx4 LOS flag mask	Masking bit for Tx LOS flag, lane 4	
	2	M-Tx3 LOS flag mask	Masking bit for Tx LOS flag, lane 3	
	1	M-Tx2 LOS flag mask	Masking bit for Tx LOS flag, lane 2	
	0	M-Tx1 LOS flag mask	Masking bit for Tx LOS flag, lane 1	
216	7	M-Tx8 CDR LOL flag mask	Masking bit for Tx CDR LOL flag, lane 8	RW Opt.
	6	M-Tx7 CDR LOL flag mask	Masking bit for Tx CDR LOL flag, lane 7	
	5	M-Tx6 CDR LOL flag mask	Masking bit for Tx CDR LOL flag, lane 6	
	4	M-Tx5 CDR LOL flag mask	Masking bit for Tx CDR LOL flag, lane 5	
	3	M-Tx4 CDR LOL flag mask	Masking bit for Tx CDR LOL flag, lane 4	
	2	M-Tx3 CDR LOL flag mask	Masking bit for Tx CDR LOL flag, lane 3	
	1	M-Tx2 CDR LOL flag mask	Masking bit for Tx CDR LOL flag, lane 2	
	0	M-Tx1 CDR LOL flag mask	Masking bit for Tx CDR LOL flag, lane 1	
217	7	M-Tx8 Adaptive Eq Fault flag mask	Masking bit for Tx Adaptive Input Eq Fault lane 8	RW Opt.
	6	M-Tx7 Adaptive Eq Fault flag mask	Masking bit for Tx Adaptive Input Eq Fault lane 7	
	5	M-Tx6 Adaptive Eq Fault flag mask	Masking bit for Tx Adaptive Input Eq Fault lane 6	
	4	M-Tx5 Adaptive Eq Fault flag mask	Masking bit for Tx Adaptive Input Eq Fault lane 5	
	3	M-Tx4 Adaptive Eq Fault flag mask	Masking bit for Tx Adaptive Input Eq Fault lane 4	
	2	M-Tx3 Adaptive Eq Fault flag mask	Masking bit for Tx Adaptive Input Eq Fault lane 3	
	1	M-Tx2 Adaptive Eq Fault flag mask	Masking bit for Tx Adaptive Input Eq Fault lane 2	

	0	M-Tx1 Adaptive Eq Fault flag mask	Masking bit for Tx Adaptive Input Eq Fault lane 1	
218	7	M-Tx8 Power High Alarm flag mask	Masking bit for Tx output power High Alarm, media lane 8	RW Opt.
	6	M-Tx7 Power High Alarm flag mask	Masking bit for Tx output power High Alarm, media lane 7	
	5	M-Tx6 Power High Alarm flag mask	Masking bit for Tx output power High Alarm, media lane 6	
	4	M-Tx5 Power High Alarm flag mask	Masking bit for Tx output power High Alarm, media lane 5	
	3	M-Tx4 Power High Alarm flag mask	Masking bit for Tx output power High Alarm, media lane 4	
	2	M-Tx3 Power High Alarm flag mask	Masking bit for Tx output power High Alarm, media lane 3	
	1	M-Tx2 Power High Alarm flag mask	Masking bit for Tx output power High Alarm, media lane 2	
	0	M-Tx1 Power High Alarm flag mask	Masking bit for Tx output power High Alarm, media lane 1	
219	7	M-Tx8 Power Low Alarm flag mask	Masking bit for Tx output power Low Alarm, media lane 8	RW Opt.
	6	M-Tx7 Power Low Alarm flag mask	Masking bit for Tx output power Low Alarm, media lane 7	
	5	M-Tx6 Power Low Alarm flag mask	Masking bit for Tx output power Low Alarm, media lane 6	
	4	M-Tx5 Power Low Alarm flag mask	Masking bit for Tx output power Low Alarm, media lane 5	
	3	M-Tx4 Power Low Alarm flag mask	Masking bit for Tx output power Low Alarm, media lane 4	
	2	M-Tx3 Power Low Alarm flag mask	Masking bit for Tx output power Low Alarm, media lane 3	
	1	M-Tx2 Power Low Alarm flag mask	Masking bit for Tx output power Low Alarm, media lane 2	
	0	M-Tx1 Power Low Alarm flag mask	Masking bit for Tx output power Low Alarm, media lane 1	
220	7	M-Tx8 Power High Warning flag mask	Masking bit for Tx output power High Warning, media lane 8	RW Opt.
	6	M-Tx7 Power High Warning flag mask	Masking bit for Tx output power High Warning, media lane 7	
	5	M-Tx6 Power High Warning flag mask	Masking bit for Tx output power High Warning, media lane 6	
	4	M-Tx5 Power High Warning flag mask	Masking bit for Tx output power High Warning, media lane 5	
	3	M-Tx4 Power High Warning flag mask	Masking bit for Tx output power High Warning, media lane 4	
	2	M-Tx3 Power High Warning flag mask	Masking bit for Tx output power High Warning, media lane 3	
	1	M-Tx2 Power High Warning flag mask	Masking bit for Tx output power High Warning, media lane 2	
	0	M-Tx1 Power High Warning flag mask	Masking bit for Tx output power High Warning, media lane 1	
221	7	M-Tx8 Power Low Warning flag mask	Masking bit for Tx output power Low Warning, media lane 8	RW Opt.
	6	M-Tx7 Power Low Warning flag mask	Masking bit for Tx output power Low Warning, media lane 7	
	5	M-Tx6 Power Low Warning flag mask	Masking bit for Tx output power Low Warning, media lane 6	
	4	M-Tx5 Power Low Warning flag mask	Masking bit for Tx output power Low Warning, media lane 5	

	3	M-Tx4 Power Low Warning flag mask	Masking bit for Tx output power Low Warning, media lane 4	
	2	M-Tx3 Power Low Warning flag mask	Masking bit for Tx output power Low Warning, media lane 3	
	1	M-Tx2 Power Low Warning flag mask	Masking bit for Tx output power Low Warning, media lane 2	
	0	M-Tx1 Power Low Warning flag mask	Masking bit for Tx output power Low Warning, media lane 1	
222	7	M-Tx8 Bias High Alarm flag mask	Masking bit for Tx bias High Alarm, media lane 8	RW Opt.
	6	M-Tx7 Bias High Alarm flag mask	Masking bit for Tx bias High Alarm, media lane 7	
	5	M-Tx6 Bias High Alarm flag mask	Masking bit for Tx bias High Alarm, media lane 6	
	4	M-Tx5 Bias High Alarm flag mask	Masking bit for Tx bias High Alarm, media lane 5	
	3	M-Tx4 Bias High Alarm flag mask	Masking bit for Tx bias High Alarm, media lane 4	
	2	M-Tx3 Bias High Alarm flag mask	Masking bit for Tx bias High Alarm, media lane 3	
	1	M-Tx2 Bias High Alarm flag mask	Masking bit for Tx bias High Alarm, media lane 2	
	0	M-Tx1 Bias High Alarm flag mask	Masking bit for Tx bias High Alarm, media lane 1	
223	7	M-Tx8 Bias Low Alarm flag mask	Masking bit for Tx bias Low Alarm, media lane 8	RW Opt.
	6	M-Tx7 Bias Low Alarm flag mask	Masking bit for Tx bias Low Alarm, media lane 7	
	5	M-Tx6 Bias Low Alarm flag mask	Masking bit for Tx bias Low Alarm, media lane 6	
	4	M-Tx5 Bias Low Alarm flag mask	Masking bit for Tx bias Low Alarm, media lane 5	
	3	M-Tx4 Bias Low Alarm flag mask	Masking bit for Tx bias Low Alarm, media lane 4	
	2	M-Tx3 Bias Low Alarm flag mask	Masking bit for Tx bias Low Alarm, media lane 3	
	1	M-Tx2 Bias Low Alarm flag mask	Masking bit for Tx Bias Low Alarm, media lane 2	
	0	M-Tx1 Bias Low Alarm flag mask	Masking bit for Tx Bias Low Alarm, media lane 1	
224	7	M-Tx8 Bias High Warning flag mask	Masking bit for Tx Bias High Warning, media lane 8	RW Opt.
	6	M-Tx7 Bias High Warning flag mask	Masking bit for Tx Bias High Warning, media lane 7	
	5	M-Tx6 Bias High Warning flag mask	Masking bit for Tx Bias High Warning, media lane 6	
	4	M-Tx5 Bias High Warning flag mask	Masking bit for Tx Bias High Warning, media lane 5	
	3	M-Tx4 Bias High Warning flag mask	Masking bit for Tx Bias High Warning, media lane 4	
	2	M-Tx3 Bias High Warning flag mask	Masking bit for Tx Bias High Warning, media lane 3	
	1	M-Tx2 Bias High Warning flag mask	Masking bit for Tx Bias High Warning, media lane 2	
	0	M-Tx1 Bias High Warning flag mask	Masking bit for Tx Bias High Warning, media lane 1	
225	7	M-Tx8 Bias Low Warning flag mask	Masking bit for Tx Bias Low Warning, media lane 8	RW Opt.

	6	M-Tx7 Bias Low Warning flag mask	Masking bit for Tx Bias Low Warning, media lane 7	
	5	M-Tx6 Bias Low Warning flag mask	Masking bit for Tx Bias Low Warning, media lane 6	
	4	M-Tx5 Bias Low Warning flag mask	Masking bit for Tx Bias Low Warning, media lane 5	
	3	M-Tx4 Bias Low Warning flag mask	Masking bit for Tx Bias Low Warning, media lane 4	
	2	M-Tx3 Bias Low Warning flag mask	Masking bit for Tx Bias Low Warning, media lane 3	
	1	M-Tx2 Bias Low Warning flag mask	Masking bit for Tx Bias Low Warning, media lane 2	
	0	M-Tx1 Bias Low Warning flag mask	Masking bit for Tx Bias Low Warning, media lane 1	
226	7	M-Rx8 LOS flag mask	Masking bit for Rx LOS flag, media lane 8	RW Opt.
	6	M-Rx7 LOS flag mask	Masking bit for Rx LOS flag, media lane 7	
	5	M-Rx6 LOS flag mask	Masking bit for Rx LOS flag, media lane 6	
	4	M-Rx5 LOS flag mask	Masking bit for Rx LOS flag, media lane 5	
	3	M-Rx4 LOS flag mask	Masking bit for Rx LOS flag, media lane 4	
	2	M-Rx3 LOS flag mask	Masking bit for Rx LOS flag, media lane 3	
	1	M-Rx2 LOS flag mask	Masking bit for Rx LOS flag, media lane 2	
	0	M-Rx1 LOS flag mask	Masking bit for Rx LOS flag, media lane 1	
227	7	M-Rx8 CDR LOL flag mask	Masking bit for Rx CDR LOL flag, media lane 8	RW Opt.
	6	M-Rx7 CDR LOL flag mask	Masking bit for Rx CDR LOL flag, media lane 7	
	5	M-Rx6 CDR LOL flag mask	Masking bit for Rx CDR LOL flag, media lane 6	
	4	M-Rx5 CDR LOL flag mask	Masking bit for Rx CDR LOL flag, media lane 5	
	3	M-Rx4 CDR LOL flag mask	Masking bit for Rx CDR LOL flag, media lane 4	
	2	M-Rx3 CDR LOL flag mask	Masking bit for Rx CDR LOL flag, media lane 3	
	1	M-Rx2 CDR LOL flag mask	Masking bit for Rx CDR LOL flag, media lane 2	
	0	M-Rx1 CDR LOL flag mask	Masking bit for Rx CDR LOL flag, media lane 1	
228	7	M-Rx8 Power High Alarm flag mask	Masking bit for Rx input power High Alarm, media lane 8	RW Opt.
	6	M-Rx7 Power High Alarm flag mask	Masking bit for Rx input power High Alarm, media lane 7	
	5	M-Rx6 Power High Alarm flag mask	Masking bit for Rx input power High Alarm, media lane 6	
	4	M-Rx5 Power High Alarm flag mask	Masking bit for Rx input power High Alarm, media lane 5	
	3	M-Rx4 Power High Alarm flag mask	Masking bit for Rx input power High Alarm, media lane 4	
	2	M-Rx3 Power High Alarm flag mask	Masking bit for Rx input power High Alarm, media lane 3	
	1	M-Rx2 Power High Alarm flag mask	Masking bit for Rx input power High Alarm, media lane 2	
	0	M-Rx1 Power High Alarm flag mask	Masking bit for Rx input power High Alarm, media lane 1	
229	7	M-Rx8 Power Low Alarm flag mask	Masking bit for Rx input power low Alarm, media lane 8	RW Opt.
	6	M-Rx7 Power Low Alarm flag mask	Masking bit for Rx input power low Alarm, media lane 7	
	5	M-Rx6 Power Low Alarm flag mask	Masking bit for Rx input power low Alarm, media lane 6	
	4	M-Rx5 Power Low Alarm flag mask	Masking bit for Rx input power low Alarm, media lane 5	
	3	M-Rx4 Power Low Alarm flag mask	Masking bit for Rx input power low Alarm, media lane 4	
	2	M-Rx3 Power Low Alarm flag mask	Masking bit for Rx input power low Alarm, media lane 3	

	1	M-Rx2 Power Low Alarm flag mask	Masking bit for Rx input power low Alarm, media lane 2	
	0	M-Rx1 Power Low Alarm flag mask	Masking bit for Rx input power low Alarm, media lane 1	
230	7	M-Rx8 Power High Warning flag mask	Masking bit for Rx input power High Warning, media lane 8	RW Opt.
	6	M-Rx7 Power High Warning flag mask	Masking bit for Rx input power High Warning, media lane 7	
	5	M-Rx6 Power High Warning flag mask	Masking bit for Rx input power High Warning, media lane 6	
	4	M-Rx5 Power High Warning flag mask	Masking bit for Rx input power High Warning, media lane 5	
	3	M-Rx4 Power High Warning flag mask	Masking bit for Rx input power High Warning, media lane 4	
	2	M-Rx3 Power High Warning flag mask	Masking bit for Rx input power High Warning, media lane 3	
	1	M-Rx2 Power High Warning flag mask	Masking bit for Rx input power High Warning, media lane 2	
	0	M-Rx1 Power High Warning flag mask	Masking bit for Rx input power High Warning, media lane 1	
231	7	M-Rx8 Power Low Warning flag mask	Masking bit for Rx input power Low Warning, media lane 8	RW Opt.
	6	M-Rx7 Power Low Warning flag mask	Masking bit for Rx input power Low Warning, media lane 7	
	5	M-Rx6 Power Low Warning flag mask	Masking bit for Rx input power Low Warning, media lane 6	
	4	M-Rx5 Power Low Warning flag mask	Masking bit for Rx input power Low Warning, media lane 5	
	3	M-Rx4 Power Low Warning flag mask	Masking bit for Rx input power Low Warning, media lane 4	
	2	M-Rx3 Power Low Warning flag mask	Masking bit for Rx input power Low Warning, media lane 3	
	1	M-Rx2 Power Low Warning flag mask	Masking bit for Rx input power Low Warning, media lane 2	
	0	M-Rx1 Power Low Warning flag mask	Masking bit for Rx input power Low Warning, media lane 1	

1.7.7 Upper Page 11h

The upper memory map page 17 is a banked page that contains lane dynamic status bytes. The presence of Upper Page 11h is conditional on the state of bit 7 in Page 00h byte 2. All fields on Upper Page 11h are read-only. Upper page 17 is subdivided into several areas as illustrated in the following table:

Table 64- Upper Page 17 Overview (Page 11h)

Byte	Size (bytes)	Name	Description
128-131	4	Datapath State indicators	
132-133	2	Reserved	
134-152	19	Lane-specific flags	
153	1	Reserved	
154-201	48	Lane-specific monitors	
202-205	4	Configuration Error Codes	Indicates validity of select Application codes
206-234	29	Active Control Set	
235-239	5	Reserved	

240-255	16	Host Electrical to Module Media Lane Mapping	Indicates the mapping of Host Electrical lanes to Module Media lanes

1.7.7.1 Data Path State Indicator

The following fields identify the Data Path State for each lane in the module. For data paths with multiple lanes, all lanes shall report the same state. An indication of DataPathDeactivated means the lane is powered down and not part of an active data path. Table 66 defines the valid Data Path State encodings.

Table 65- Data Path State Indicator, per lane (Page 11h) (see Table 66)

Byte	Bit	Name	Description	Type
128	7-4	Lane 2 Data Path State	Data path state encoding for lane 2	RO
	3-0	Lane 1 Data Path State	Data path state encoding for lane 1	RQD
129	7-4	Lane 4 Data Path State	Data path state encoding for lane 4	RO
	3-0	Lane 3 Data Path State	Data path state encoding for lane 3	RQD
130	7-4	Lane 6 Data Path State	Data path state encoding for lane 6	RO
	3-0	Lane 5 Data Path State	Data path state encoding for lane 5	RQD
131	7-4	Lane 8 Data Path State	Data path state encoding for lane 8	RO
	3-0	Lane 7 Data Path State	Data path state encoding for lane 7	RQD

Table 66- Data Path State Indicator Encodings

Encoding	State
0h	Reserved
1h	DataPathDeactivated State
2h	DataPathInit State
3h	DataPathDeinit State
4h	DataPathActivated State
5h-Fh	Reserved

1.7.7.2 Lane-Specific Flags

This section of the memory map contains lane-specific flags. These flags provide a mechanism for reporting lane-specific alarms and warnings for fault conditions. If a lane-specific flag with associated alarm and/or warning thresholds is implemented the associated flags and flag masks must also be implemented. For normal operation and default state, the bits in this field have the value of 0b. Once asserted, the bits remain set (latched) until cleared by a read operation that includes the affected bit or reset by the Reset signal. Note that a read of the flag summary shall not clear the underlying flag condition. If the corresponding mask bit is not set (see Table 63), Interrupt is also asserted at the onset of the condition and remains asserted until all asserted flags (both module-level and lane-specific) have been cleared by a host read. After being read and cleared, the bit shall be set again if the condition persists; this will cause Interrupt to be asserted again unless masked. The lane-specific flags are defined in Table 68 and Table 69.

Table 67- Lane-Specific State Changed Flags (Page 11h)

Byte	Bit	Name	Description	Type
134	7	L-Lane 8 Data Path State Changed flag	Latched Data Path State Changed flag for lane 8	RO RQD
	6	L-Lane 7 Data Path State changed flag	Latched Data Path State Changed flag for lane 7	
	5	L-Lane 6 Data Path State Changed flag	Latched Data Path State Changed flag for lane 6	

	4	L-Lane 5 Data Path State Changed flag	Latched Data Path State Changed flag for lane 5	
	3	L-Lane 4 Data Path State Changed flag	Latched Data Path State Changed flag for lane 4	
	2	L-Lane 3 Data Path State Changed flag	Latched Data Path State Changed flag for lane 3	
	1	L-Lane 2 Data Path State Changed flag	Latched Data Path State Changed flag for lane 2	
	0	L-Lane 1 Data Path State Changed flag	Latched Data Path State Changed flag for lane 1	

Table 68- Lane-Specific TX Flags (Page 11h)

Byte	Bit	Name	Description	Type
135	7	L-Tx8 Fault flag	Latched Tx Fault flag, media lane 8	RO Opt.
	6	L-Tx7 Fault flag	Latched Tx Fault flag, media lane 7	
	5	L-Tx6 Fault flag	Latched Tx Fault flag, media lane 6	
	4	L-Tx5 Fault flag	Latched Tx Fault flag, media lane 5	
	3	L-Tx4 Fault flag	Latched Tx Fault flag, media lane 4	
	2	L-Tx3 Fault flag	Latched Tx Fault flag, media lane 3	
	1	L-Tx2 Fault flag	Latched Tx Fault flag, media lane 2	
	0	L-Tx1 Fault flag	Latched Tx Fault flag, media lane 1	
136	7	L-Tx8 LOS flag	Latched Tx LOS flag, lane 8	RO Opt.
	6	L-Tx7 LOS flag	Latched Tx LOS flag, lane 7	
	5	L-Tx6 LOS flag	Latched Tx LOS flag, lane 6	
	4	L-Tx5 LOS flag	Latched Tx LOS flag, lane 5	
	3	L-Tx4 LOS flag	Latched Tx LOS flag, lane 4	
	2	L-Tx3 LOS flag	Latched Tx LOS flag, lane 3	
	1	L-Tx2 LOS flag	Latched Tx LOS flag, lane 2	
	0	L-Tx1 LOS flag	Latched Tx LOS flag, lane 1	
137	7	L-Tx8 CDR LOL flag	Latched Tx CDR LOL flag, lane 8	RO Opt.
	6	L-Tx7 CDR LOL flag	Latched Tx CDR LOL flag, lane 7	
	5	L-Tx6 CDR LOL flag	Latched Tx CDR LOL flag, lane 6	
	4	L-Tx5 CDR LOL flag	Latched Tx CDR LOL flag, lane 5	
	3	L-Tx4 CDR LOL flag	Latched Tx CDR LOL flag, lane 4	
	2	L-Tx3 CDR LOL flag	Latched Tx CDR LOL flag, lane 3	
	1	L-Tx2 CDR LOL flag	Latched Tx CDR LOL flag, lane 2	
	0	L-Tx1 CDR LOL flag	Latched Tx CDR LOL flag, lane 1	
138	7	L-Tx Adaptive Input Eq Fault Lane 8 flag	Latched Tx Adaptive Input Eq. Fault Lane 8	RO Opt.
	6	L-Tx Adaptive Input Eq Fault Lane 7 flag	Latched Tx Adaptive Input Eq. Fault Lane 7	
	5	L-Tx Adaptive Input Eq Fault Lane 6 flag	Latched Tx Adaptive Input Eq. Fault Lane 6	
	4	L-Tx Adaptive Input Eq Fault Lane 5 flag	Latched Tx Adaptive Input Eq. Fault Lane 5	
	3	L-Tx Adaptive Input Eq Fault Lane 4 flag	Latched Tx Adaptive Input Eq. Fault Lane 4	
	2	L-Tx Adaptive Input Eq Fault Lane 3 flag	Latched Tx Adaptive Input Eq. Fault Lane 3	
	1	L-Tx Adaptive Input Eq Fault Lane 2 flag	Latched Tx Adaptive Input Eq. Fault Lane 2	
	0	L-Tx Adaptive Input Eq Fault Lane 1 flag	Latched Tx Adaptive Input Eq. Fault Lane 1	
139	7	L-Tx8 Power High alarm	Tx output power High Alarm, media lane 8	RO Opt.
	6	L-Tx7 Power High alarm	Tx output power High Alarm, media lane 7	
	5	L-Tx6 Power High alarm	Tx output power High Alarm, media lane 6	

	4	L-Tx5 Power High alarm	Tx output power High Alarm, media lane 5	
	3	L-Tx4 Power High alarm	Tx output power High Alarm, media lane 4	
	2	L-Tx3 Power High alarm	Tx output power High Alarm, media lane 3	
	1	L-Tx2 Power High alarm	Tx output power High Alarm, media lane 2	
	0	L-Tx1 Power High alarm	Tx output power High Alarm, media lane 1	
140	7	L-Tx8 Power Low alarm	Tx output power Low alarm, media lane 8	RO Opt.
	6	L-Tx7 Power Low alarm	Tx output power Low alarm, media lane 7	
	5	L-Tx6 Power Low alarm	Tx output power Low alarm, media lane 6	
	4	L-Tx5 Power Low alarm	Tx output power Low alarm, media lane 5	
	3	L-Tx4 Power Low alarm	Tx output power Low alarm, media lane 4	
	2	L-Tx3 Power Low alarm	Tx output power Low alarm, media lane 3	
	1	L-Tx2 Power Low alarm	Tx output power Low alarm, media lane 2	
	0	L-Tx1 Power Low alarm	Tx output power Low alarm, media lane 1	
141	7	L-Tx8 Power High warning	Tx output power High warning, media lane 8	RO Opt.
	6	L-Tx7 Power High warning	Tx output power High warning, media lane 7	
	5	L-Tx6 Power High warning	Tx output power High warning, media lane 6	
	4	L-Tx5 Power High warning	Tx output power High warning, media lane 5	
	3	L-Tx4 Power High warning	Tx output power High warning, media lane 4	
	2	L-Tx3 Power High warning	Tx output power High warning, media lane 3	
	1	L-Tx2 Power High warning	Tx output power High warning, media lane 2	
	0	L-Tx1 Power High warning	Tx output power High warning, media lane 1	
142	7	L-Tx8 Power Low warning	Tx output power Low warning, media lane 8	RO Opt.
	6	L-Tx7 Power Low warning	Tx output power Low warning, media lane 7	
	5	L-Tx6 Power Low warning	Tx output power Low warning, media lane 6	
	4	L-Tx5 Power Low warning	Tx output power Low warning, media lane 5	
	3	L-Tx4 Power Low warning	Tx output power Low warning, media lane 4	
	2	L-Tx3 Power Low warning	Tx output power Low warning, media lane 3	
	1	L-Tx2 Power Low warning	Tx output power Low warning, media lane 2	
	0	L-Tx1 Power Low warning	Tx output power Low warning, media lane 1	
143	7	L-Tx8 Bias High Alarm	Tx Bias High Alarm, media lane 8	RO Opt.
	6	L-Tx7 Bias High Alarm	Tx Bias High Alarm, media lane 7	
	5	L-Tx6 Bias High Alarm	Tx Bias High Alarm, media lane 6	
	4	L-Tx5 Bias High Alarm	Tx Bias High Alarm, media lane 5	
	3	L-Tx4 Bias High Alarm	Tx Bias High Alarm, media lane 4	
	2	L-Tx3 Bias High Alarm	Tx Bias High Alarm, media lane 3	
	1	L-Tx2 Bias High Alarm	Tx Bias High Alarm, media lane 2	
	0	L-Tx1 Bias High Alarm	Tx Bias High Alarm, media lane 1	
144	7	L-Tx8 Bias Low alarm	Tx Bias Low alarm, media lane 8	RO Opt.
	6	L-Tx7 Bias Low alarm	Tx Bias Low alarm, media lane 7	
	5	L-Tx6 Bias Low alarm	Tx Bias Low alarm, media lane 6	
	4	L-Tx5 Bias Low alarm	Tx Bias Low alarm, media lane 5	
	3	L-Tx4 Bias Low alarm	Tx Bias Low alarm, media lane 4	

	2	L-Tx3 Bias Low alarm	Tx Bias Low alarm, media lane 3	
	1	L-Tx2 Bias Low alarm	Tx Bias Low alarm, media lane 2	
	0	L-Tx1 Bias Low alarm	Tx Bias Low alarm, media lane 1	
145	7	L-Tx8 Bias High warning	Tx Bias High warning, media lane 8	RO Opt.
	6	L-Tx7 Bias High warning	Tx Bias High warning, media lane 7	
	5	L-Tx6 Bias High warning	Tx Bias High warning, media lane 6	
	4	L-Tx5 Bias High warning	Tx Bias High warning, media lane 5	
	3	L-Tx4 Bias High warning	Tx Bias High warning, media lane 4	
	2	L-Tx3 Bias High warning	Tx Bias High warning, media lane 3	
	1	L-Tx2 Bias High warning	Tx Bias High warning, media lane 2	
	0	L-Tx1 Bias High warning	Tx Bias High warning, media lane 1	
146	7	L-Tx8 Bias Low warning	Tx Bias Low warning, media lane 8	RO Opt.
	6	L-Tx7 Bias Low warning	Tx Bias Low warning, media lane 7	
	5	L-Tx6 Bias Low warning	Tx Bias Low warning, media lane 6	
	4	L-Tx5 Bias Low warning	Tx Bias Low warning, media lane 5	
	3	L-Tx4 Bias Low warning	Tx Bias Low warning, media lane 4	
	2	L-Tx3 Bias Low warning	Tx Bias Low warning, media lane 3	
	1	L-Tx2 Bias Low warning	Tx Bias Low warning, media lane 2	
	0	L-Tx1 Bias Low warning	Tx Bias Low warning, media lane 1	

Table 69- RX Flags (Page 11h, active modules only)

Byte	Bit	Name	Description	Type
147	7	L-Rx8 LOS	Latched Rx LOS flag, media lane 8	RO Opt.
	6	L-Rx7 LOS	Latched Rx LOS flag, media lane 7	
	5	L-Rx6 LOS	Latched Rx LOS flag, media lane 6	
	4	L-Rx5 LOS	Latched Rx LOS flag, media lane 5	
	3	L-Rx4 LOS	Latched Rx LOS flag, media lane 4	
	2	L-Rx3 LOS	Latched Rx LOS flag, media lane 3	
	1	L-Rx2 LOS	Latched Rx LOS flag, media lane 2	
	0	L-Rx1 LOS	Latched Rx LOS flag, media lane 1	
148	7	L-Rx8 CDR LOL	Latched Rx CDR LOL flag, media lane 8	RO Opt.
	6	L-Rx7 CDR LOL	Latched Rx CDR LOL flag, media lane 7	
	5	L-Rx6 CDR LOL	Latched Rx CDR LOL flag, media lane 6	
	4	L-Rx5 CDR LOL	Latched Rx CDR LOL flag, media lane 5	
	3	L-Rx4 CDR LOL	Latched Rx CDR LOL flag, media lane 4	
	2	L-Rx3 CDR LOL	Latched Rx CDR LOL flag, media lane 3	
	1	L-Rx2 CDR LOL	Latched Rx CDR LOL flag, media lane 2	
	0	L-Rx1 CDR LOL	Latched Rx CDR LOL flag, media lane 1	
149	7	L-Rx8 Power High alarm	Rx input power High alarm, media lane 8	RO Opt.
	6	L-Rx7 Power High alarm	Rx input power High alarm, media lane 7	
	5	L-Rx6 Power High alarm	Rx input power High alarm, media lane 6	
	4	L-Rx5 Power High alarm	Rx input power High alarm, media lane 5	
	3	L-Rx4 Power High alarm	Rx input power High alarm, media lane 4	
	2	L-Rx3 Power High alarm	Rx input power High alarm, media lane 3	
	1	L-Rx2 Power High alarm	Rx input power High alarm, media lane 2	
	0	L-Rx1 Power High alarm	Rx input power High alarm, media lane 1	
150	7	L-Rx8 Power Low alarm	Rx input power Low alarm, media lane 8	RO Opt.
	6	L-Rx7 Power Low alarm	Rx input power Low alarm, media lane 7	

	5	L-Rx6 Power Low alarm	Rx input power Low alarm, media lane 6	
	4	L-Rx5 Power Low alarm	Rx input power Low alarm, media lane 5	
	3	L-Rx4 Power Low alarm	Rx input power Low alarm, media lane 4	
	2	L-Rx3 Power Low alarm	Rx input power Low alarm, media lane 3	
	1	L-Rx2 Power Low alarm	Rx input power Low alarm, media lane 2	
	0	L-Rx1 Power Low alarm	Rx input power Low alarm, media lane 1	
151	7	L-Rx8 Power High warning	Rx input power High warning, media lane 8	RO Opt.
	6	L-Rx7 Power High warning	Rx input power High warning, media lane 7	
	5	L-Rx6 Power High warning	Rx input power High warning, media lane 6	
	4	L-Rx5 Power High warning	Rx input power High warning, media lane 5	
	3	L-Rx4 Power High warning	Rx input power High warning, media lane 4	
	2	L-Rx3 Power High warning	Rx input power High warning, media lane 3	
	1	L-Rx2 Power High warning	Rx input power High warning, media lane 2	
	0	L-Rx1 Power High warning	Rx input power High warning, media lane 1	
152	7	L-Rx8 Power Low warning	Rx input power Low warning, media lane 8	RO Opt.
	6	L-Rx7 Power Low warning	Rx input power Low warning, media lane 7	
	5	L-Rx6 Power Low warning	Rx input power Low warning, media lane 6	
	4	L-Rx5 Power Low warning	Rx input power Low warning, media lane 5	
	3	L-Rx4 Power Low warning	Rx input power Low warning, media lane 4	
	2	L-Rx3 Power Low warning	Rx input power Low warning, media lane 3	
	1	L-Rx2 Power Low warning	Rx input power Low warning, media lane 2	
	0	L-Rx1 Power Low warning	Rx input power Low warning, media lane 1	

1.7.7.3 Lane-Specific Monitors

Real time lane monitoring may be performed for each transmit and receive lane and includes Tx output optical power, Rx input optical power, and Tx bias current. Alarm threshold values and warning threshold values have the same numerical value representation as the associated monitor values for which they specify threshold values.

Measured TX bias current is represented as a 16-bit unsigned integer with the current defined as the full 16-bit value (0 to 65535) with LSB equal to 2 uA times the multiplier from page 01h byte 160. For a multiplier of 1, this yields a total measurement range of 0 to 131 mA. Accuracy is Vendor Specific but must be better than +/-10% of the manufacturer's nominal value over specified operating temperature and voltage.

Measured RX input optical power is in mW and can represent either average received power or OMA depending the Rx Optical Power Measurement type in Table 42. The parameter is encoded as a 16-bit unsigned integer with the power defined as the full 16-bit value (0 to 65535) with LSB equal to 0.1 uW, yielding a total measurement range of 0 to 6.5535 mW (~-40 to +8.2 dBm). Absolute accuracy is dependent upon the exact optical wavelength. For the vendor specified wavelength, accuracy shall be better than +/-3 dB over specified temperature and voltage. This accuracy shall be maintained for input power levels up to the lesser of maximum transmitted or maximum received optical power per the appropriate standard. It shall be maintained down to the minimum transmitted power minus cable plant loss (insertion loss or passive loss) per the appropriate standard. Absolute accuracy beyond this minimum required received input optical power range is Vendor Specific.

Measured TX optical power is the average power represented in mW. The parameter is encoded as a 16-bit unsigned integer with the power defined as the full 16-bit value (0 to 65535) with LSB equal to 0.1 uW, yielding a total measurement range of 0 to 6.5535 mW (~-40 to +8.2 dBm). For the vendor specified wavelength, accuracy shall be better than +/-3 dB over specified temperature and voltage.

Table 70- Lane-Specific Monitors (Page 11h, active modules only)

Byte	Bit	Name	Description	Type
153	7-0	Reserved		RO
154	7-0	Tx1 Power MSB	Internally measured Tx output optical power:	RO

155	7-0	Tx1 Power LSB	unsigned integer in 0.1 uW increments, yielding a total measurement range of 0 to 6.5535 mW (~-40 to +8.2 dBm)	Opt.
156	7-0	Tx2 Power MSB		
157	7-0	Tx2 Power LSB		
158	7-0	Tx3 Power MSB		
159	7-0	Tx3 Power LSB		
160	7-0	Tx4 Power MSB		
161	7-0	Tx4 Power LSB		
162	7-0	Tx5 Power MSB		
163	7-0	Tx5 Power LSB		
164	7-0	Tx6 Power MSB		
165	7-0	Tx6 Power LSB		
166	7-0	Tx7 Power MSB		
167	7-0	Tx7 Power LSB		
168	7-0	Tx8 Power MSB		
169	7-0	Tx8 Power LSB		
170	7-0	Tx1 Bias MSB	Internally measured Tx bias current monitor: unsigned integer in 2 uA increments, times the multiplier from Table 45.	RO Opt.
171	7-0	Tx1 Bias LSB		
172	7-0	Tx2 Bias MSB		
173	7-0	Tx2 Bias LSB		
174	7-0	Tx3 Bias MSB		
175	7-0	Tx3 Bias LSB		
176	7-0	Tx4 Bias MSB		
177	7-0	Tx4 Bias LSB		
178	7-0	Tx5 Bias MSB		
179	7-0	Tx5 Bias LSB		
180	7-0	Tx6 Bias MSB		
181	7-0	Tx6 Bias LSB		
182	7-0	Tx7 Bias MSB		
183	7-0	Tx7 Bias LSB		
184	7-0	Tx8 Bias MSB		
185	7-0	Tx8 Bias LSB		
186	7-0	Rx1 Power MSB	Internally measured Rx input optical power: unsigned integer in 0.1 uW increments, yielding a total measurement range of 0 to 6.5535 mW (~-40 to +8.2 dBm)	RO Opt.
187	7-0	Rx1 Power LSB		
188	7-0	Rx2 Power MSB		
189	7-0	Rx2 Power LSB		
190	7-0	Rx3 Power MSB		
191	7-0	Rx3 Power LSB		
192	7-0	Rx4 Power MSB		
193	7-0	Rx4 Power LSB		
194	7-0	Rx5 Power MSB		
195	7-0	Rx5 Power LSB		
196	7-0	Rx6 Power MSB		
197	7-0	Rx6 Power LSB		
198	7-0	Rx7 Power MSB		
199	7-0	Rx7 Power LSB		
200	7-0	Rx8 Power MSB		
201	7-0	Rx8 Power LSB		

1.7.7.4 Configuration Error Codes

The configuration requested by the host in either Staged Set may not be supported by the module for a variety of reasons. The Configuration Error Code registers are defined to provide feedback to the host software for cases where an invalid configuration was requested.

A code is provided for each lane (see Table 71). In cases where the feedback is data path-wide, the module shall populate all lanes in the data path with the same code. The

applicable Configuration Error Code registers shall be populated by the module when the host sets one or more bits in Apply_DataPathInit or Apply_Immediate, before the requested configuration is copied into the Active Set. If the configuration was determined to be invalid by the module, the configuration shall not be copied into the Active Set. Any configuration error code greater than or equal to 2 indicates a rejected configuration.

Table 71- Configuration Error Code registers (Page 11h, active modules only)

Byte	Bit	Name	Description	Type
202	7-4	Lane 2 Config Error Code	Configuration Error Code for lane 2	RO Opt.
	3-0	Lane 1 Config Error Code	Configuration Error Code for lane 1	
203	7-4	Lane 4 Config Error Code	Configuration Error Code for lane 4	RO Opt.
	3-0	Lane 3 Config Error Code	Configuration Error Code for lane 3	
204	7-4	Lane 6 Config Error Code	Configuration Error Code for lane 6	RO Opt.
	3-0	Lane 5 Config Error Code	Configuration Error Code for lane 5	
205	7-4	Lane 8 Config Error Code	Configuration Error Code for lane 8	RO Opt.
	3-0	Lane 7 Config Error Code	Configuration Error Code for lane 7	

Table 72- Configuration Error Codes (Page 11h, active modules only)

Encoding	Name	Description
0h	No status	No status information available or config in process
1h	Config accepted	Configuration accepted and successfully applied
2h	Config rejected unknown	Configuration rejected for unknown reason
3h	Config rejected invalid code	Configuration rejected due to invalid ApSel Code request
4h	Config rejected invalid combo	Configuration rejected due to ApSel Code requested on invalid lane combination
5h	Config rejected invalid SI	Configuration rejected due to Invalid SI control set request
6h	Config rejected in use	Configuration rejected due to portion of lane group currently in use for a different Application (in order to switch to an Application with a different lane width, all lanes in the target Data Path must be in DataPathDeactivated)
7h	Config rejected incomplete lane info	DataPathInit requested with incomplete lane information
8h-Ch	Reserved	
Dh-Fh	Custom	Configuration rejected for custom reason

1.7.7.5 Active Control Set

The Active Control Set is required for all modules. Refer to Section 1.5.4 for background on Control Set methodology.

At power on or exit from reset, the Active Control Set may be populated with a default Application Code and signal integrity settings. The host may update the Active Control Set by using the Apply_DataPathInit or Apply_Immediate control fields in either Staged Set 0 or Staged Set 1. See Section 1.7.6.3 for a description of Control Set usage.

The following fields allow the host to view the current signaling rate, modulation format, and data path width for each lane in the module.

The ApSel Code shall be one of the module-advertised ApSel Codes from Table 26 or Table 48. The Data Path code identifies the first lane in the data path. For example, a data path including lane 1 would be coded 000b and a data path where lane 5 is the lower lane

number would be coded 100b. Explicit Control (bit 0 in bytes 206-213) indicates the host has specified signal integrity settings rather than using the Application-defined settings.

Table 73- Indicators for Active Control Set, Application Selected (Page 11h, active modules only)

Byte	Bits	Name	Description	Type
206	7-4	Active Set Lane 1 Application code	ApSel Code from Table 26 or Table 48, lane 1	RO RQD
	3-1	Active Set Lane 1 Data Path code	First lane in the data path containing lane 1 000b=Lane 1	
	0	Active Set Lane 1 Explicit Control	0b=Lane 1 settings are Application-defined 1b=Lane 1 settings are host-specified	
207	7-4	Active Set Lane 2 Application code	ApSel Code from Table 26 or Table 48, lane 2	RO RQD
	3-1	Active Set Lane 2 Data Path code	First lane in the data path containing lane 2 000b=Lane 1, 001b=Lane 2	
	0	Active Set Lane 2 Explicit Control	0b=Lane 2 settings are Application-defined 1b=Lane 2 settings are host-specified	
208	7-4	Active Set Lane 3 Application code	ApSel Code from Table 26 or Table 48, lane 3	RO RQD
	3-1	Active Set Lane 3 Data Path code	First lane in the data path containing lane 3 000b=Lane 1, 001b=Lane 2, etc.	
	0	Active Set Lane 3 Explicit Control	0b=Lane 3 settings are Application-defined 1b=Lane 3 settings are host-specified	
209	7-4	Active Set Lane 4 Application code	ApSel Code from Table 26 or Table 48, lane 4	RO RQD
	3-1	Active Set Lane 4 Data Path code	First lane in the data path containing lane 4 000b=Lane 1, 001b=Lane 2, etc.	
	0	Active Set Lane 4 Explicit Control	0b=Lane 4 settings are Application-defined 1b=Lane 4 settings are host-specified	
210	7-4	Active Set Lane 5 Application code	ApSel Code from Table 26 or Table 48, lane 5	RO RQD
	3-1	Active Set Lane 5 Data Path code	First lane in the data path containing lane 5 000b=Lane 1, 001b=Lane 2, etc.	
	0	Active Set Lane 5 Explicit Control	0b=Lane 5 settings are Application-defined 1b=Lane 5 settings are host-specified	
211	7-4	Active Set Lane 6 Application code	ApSel Code from Table 26 or Table 48, lane 6	RO RQD
	3-1	Active Set Lane 6 Data Path code	First lane in the data path containing lane 6 000b=Lane 1, 001b=Lane 2, etc.	
	0	Active Set Lane 6 Explicit Control	0b=Lane 6 settings are Application-defined 1b=Lane 6 settings are host-specified	
212	7-4	Active Set Lane 7 Application code	ApSel Code from Table 26 or Table 48, lane 7	RO RQD
	3-1	Active Set Lane 7 Data Path code	First lane in the data path containing lane 7 000b=Lane 1, 001b=Lane 2, etc.	
	0	Active Set Lane 7 Explicit Control	0b=Lane 7 settings are Application-defined 1b=Lane 7 settings are host-specified	
213	7-4	Active Set Lane 8 Application code	ApSel Code from Table 26 or Table 48, lane 8	RO RQD
	3-1	Active Set Lane 8 Data Path code	First lane in the data path containing lane 8 000b=Lane 1, 001b=Lane 2, etc.	
	0	Active Set Lane 8 Explicit Control	0b=Lane 8 settings are Application-defined 1b=Lane 8 settings are host-specified	

The following fields allow the host to view the signal integrity settings for a lane. If the Explicit Control bit for a lane is set, the module is using the host-defined settings from Table 74 and Table 75. If the Explicit Control bit for a lane is clear, the module

is using Application-defined default signal integrity settings. See section 1.5.5 for definitions of valid signal integrity control settings.

Table 74- Indicators for Active Control Set, Tx Controls (Page 11h, active modules only)

Byte	Bits	Name	Description	Type
214	7	Active Set Tx8 Adaptive Input Eq Enable	1b=Enable 0b=Disable (use manual fixed EQ) See Byte 220 Page 11h	RO Opt.
	6	Active Set Tx7 Adaptive Input Eq Enable	1b=Enable 0b=Disable (use manual fixed EQ) See Byte 220 Page 11h	
	5	Active Set Tx6 Adaptive Input Eq Enable	1b=Enable 0b=Disable (use manual fixed EQ) See Byte 219 Page 11h	
	4	Active Set Tx5 Adaptive Input Eq Enable	1b=Enable 0b=Disable (use manual fixed EQ) See Byte 219 Page 11h	
	3	Active Set Tx4 Adaptive Input Eq Enable	1b=Enable 0b=Disable (use manual fixed EQ) See Byte 218 Page 11h	
	2	Active Set Tx3 Adaptive Input Eq Enable	1b=Enable 0b=Disable (use manual fixed EQ) See Byte 218 Page 11h	
	1	Active Set Tx2 Adaptive Input Eq Enable	1b=Enable 0b=Disable (use manual fixed EQ) See Byte 217 Page 11h	
	0	Active Set Tx1 Adaptive Input Eq Enable	1b=Enable 9 0b=Disable (use manual fixed EQ) See Byte 217 Page 11h	
215	7-6	Active Set Tx4 Adaptive Input Eq Recall	Recall stored Tx Eq adaptation value, 00b=do not recall 01b=store location 1 10b=store location 2 11b=reserved See Table 57 and Table 61	RO Opt.
	5-4	Active Set Tx3 Adaptive Input Eq Recall		
	3-2	Active Set Tx2 Adaptive Input Eq Recall		
	1-0	Active Set Tx1 Adaptive Input Eq Recall		
216	7-6	Active Set Tx8 Adaptive Input Eq Recall	Recall stored Tx Eq adaptation value, 00b=do not recall 01b=store location 1 10b=store location 2 11b=reserved See Table 57 and Table 61	RO Opt.
	5-4	Active Set Tx7 Adaptive Input Eq Recall		
	3-2	Active Set Tx6 Adaptive Input Eq Recall		
	1-0	Active Set Tx5 Adaptive Input Eq Recall		
217	7-4	Active Set Tx2 Input Eq control	Manual fixed Tx input eq control See Table 12	RO Opt.
	3-0	Active Set Tx1 Input Eq control	Manual fixed Tx input eq control See Table 12	
218	7-4	Active Set Tx4 Input Eq control	Manual fixed Tx input eq control See Table 12	RO Opt.
	3-0	Active Set Tx3 Input Eq control	Manual fixed Tx input eq control See Table 12	
219	7-4	Active Set Tx6 Input Eq control	Manual fixed Tx input eq control See Table 12	RO Opt.
	3-0	Active Set Tx5 Input Eq control	Manual fixed Tx input eq control See Table 12	

220	7-4	Active Set Tx8 Input Eq control	Manual fixed Tx input eq control See Table 12	RO Opt.
	3-0	Active Set Tx7 Input Eq control	Manual fixed Tx input eq control See Table 12	
221	7	Active Set Tx8 CDR control	1b=CDR enabled, 0b=CDR bypassed	RO Opt.
	6	Active Set Tx7 CDR control	1b=CDR enabled, 0b=CDR bypassed	
	5	Active Set Tx6 CDR control	1b=CDR enabled, 0b=CDR bypassed	
	4	Active Set Tx5 CDR control	1b=CDR enabled, 0b=CDR bypassed	
	3	Active Set Tx4 CDR control	1b=CDR enabled, 0b=CDR bypassed	
	2	Active Set Tx3 CDR control	1b=CDR enabled, 0b=CDR bypassed	
	1	Active Set Tx2 CDR control	1b=CDR enabled, 0b=CDR bypassed	
	0	Active Set Tx1 CDR control	1b=CDR enabled, 0b=CDR bypassed	

Table 75- Indicators for Active Control Set, Rx Controls (Page 11h, active modules only)

Byte	Bits	Name	Description	Type
222	7	Active Set Rx8 CDR control	1b=CDR enabled, 0b=CDR bypassed	RO Opt.
	6	Active Set Rx7 CDR control	1b=CDR enabled, 0b=CDR bypassed	
	5	Active Set Rx6 CDR control	1b=CDR enabled, 0b=CDR bypassed	
	4	Active Set Rx5 CDR control	1b=CDR enabled, 0b=CDR bypassed	
	3	Active Set Rx4 CDR control	1b=CDR enabled, 0b=CDR bypassed	
	2	Active Set Rx3 CDR control	1b=CDR enabled, 0b=CDR bypassed	
	1	Active Set Rx2 CDR control	1b=CDR enabled, 0b=CDR bypassed	
	0	Active Set Rx1 CDR control	1b=CDR enabled, 0b=CDR bypassed	
223	7-4	Active Set Rx2 Output Eq control, pre-cursor	Rx output equalization pre-cursor See Table 13	RO Opt.
	3-0	Active Set Rx1 Output Eq control, pre-cursor	Rx output equalization pre-cursor See Table 13	
224	7-4	Active Set Rx4 Output Eq control, pre-cursor	Rx output equalization pre-cursor See Table 13	RO Opt.
	3-0	Active Set Rx3 Output Eq control, pre-cursor	Rx output equalization pre-cursor See Table 13	
225	7-4	Active Set Rx6 Output Eq control, pre-cursor	Rx output equalization pre-cursor See Table 13	RO Opt.
	3-0	Active Set Rx5 Output Eq control, pre-cursor	Rx output equalization pre-cursor See Table 13	
226	7-4	Active Set Rx8 Output Eq control, pre-cursor	Rx output equalization pre-cursor See Table 13	RO Opt.
	3-0	Active Set Rx7 Output Eq control, pre-cursor	Rx output equalization pre-cursor See Table 13	
227	7-4	Active Set Rx2 Output Eq control, post-cursor	Rx output equalization post-cursor See Table 13	RO Opt.
	3-0	Active Set Rx1 Output Eq control, post-cursor	Rx output equalization post-cursor See Table 13	
228	7-4	Active Set Rx4 Output Eq control, post-cursor	Rx output equalization post-cursor See Table 13	RO Opt.
	3-0	Active Set Rx3 Output Eq control, post-cursor	Rx output equalization post-cursor See Table 13	
229	7-4	Active Set Rx6 Output Eq control, post-cursor	Rx output equalization post-cursor See Table 13	RO Opt.

	3-0	Active Set Rx5 Output Eq control, post-cursor	Rx output equalization post-cursor See Table 13	
230	7-4	Active Set Rx8 Output Eq control, post-cursor	Rx output equalization post-cursor See Table 13	RO Opt.
	3-0	Active Set Rx7 Output Eq control, post-cursor	Rx output equalization post-cursor See Table 13	
231	7-4	Active Set Rx2 Output Amplitude control	Rx output amplitude encoding See Table 14	RO Opt.
	3-0	Active Set Rx1 Output Amplitude control	Rx output amplitude encoding See Table 14	
232	7-4	Active Set Rx4 Output Amplitude control	Rx output amplitude encoding See Table 14	RO Opt.
	3-0	Active Set Rx3 Output Amplitude control	Rx output amplitude encoding See Table 14	
233	7-4	Active Set Rx6 Output Amplitude control	Rx output amplitude encoding See Table 14	RO Opt.
	3-0	Active Set Rx5 Output Amplitude control	Rx output amplitude encoding See Table 14	
234	7-4	Active Set Rx8 Output Amplitude control	Rx output amplitude encoding See Table 14	RO Opt.
	3-0	Active Set Rx7 Output Amplitude control	Rx output amplitude encoding See Table 14	
235-239		Reserved		RO

1.7.7.6 Module Media Lane to Module Media Wavelength and Fiber Mapping

Table 76 contains the advertising fields to define the mapping of module media lanes to module media wavelengths and physical fibers for muxed or WDM implementations. For WDM applications the shortest wavelength is always designated media wavelength 1 and starting from shortest wavelength through the longest all others are listed consecutively. The fiber numbers and names used in Table 76 are as defined in the appropriate hardware specification. See the relevant hardware specification and Table 26, Table 35 and Table 36 within for mapping constraints. Any mapping advertised in Table 76 that violates any of these constraints will not be a valid mapping. Refer to Section 1.5.2 for details.

Table 76- Module Media Lane to Module Media Wavelength and Fiber mapping (Page 11h, active modules only)

Byte	Bits	Name	Description	Type
240	7-4	Module TX media lane 1 wavelength mapping	0000= Mapping unknown or undefined 0001= Maps to module media wavelength 1 0010= Maps to module media wavelength 2 0011= Maps to module media wavelength 3 0100= Maps to module media wavelength 4 0101= Maps to module media wavelength 5 0110= Maps to module media wavelength 6 0111= Maps to module media wavelength 7 1000= Maps to module media wavelength 8 1001-1111= Reserved	RO Opt.
	3-0	Module TX media lane 1 fiber mapping	0000= Mapping unknown or undefined 0001= Maps to module media fiber 1 or TR1 0010= Maps to module media fiber 2 or RT1 0011= Maps to module media fiber 3 or TR2 0100= Maps to module media fiber 4 or RT2 0101= Maps to module media fiber 5 or TR3 0110= Maps to module media fiber 6 or RT3 0111= Maps to module media fiber 7 or TR4 1000= Maps to module media fiber 8 or RT4 1001-1111= Reserved	
241	7-4	Module TX media lane 2 wavelength mapping	0000= Mapping unknown or undefined 0001= Maps to module media wavelength 1 0010= Maps to module media wavelength 2 0011= Maps to module media wavelength 3 0100= Maps to module media wavelength 4 0101= Maps to module media wavelength 5 0110= Maps to module media wavelength 6 0111= Maps to module media wavelength 7 1000= Maps to module media wavelength 8 1001-1111= Reserved	RO Opt.
	3-0	Module TX media lane 2 fiber mapping	0000= Mapping unknown or undefined 0001= Maps to module media fiber 1 or TR1 0010= Maps to module media fiber 2 or RT1 0011= Maps to module media fiber 3 or TR2 0100= Maps to module media fiber 4 or RT2 0101= Maps to module media fiber 5 or TR3 0110= Maps to module media fiber 6 or RT3 0111= Maps to module media fiber 7 or TR4 1000= Maps to module media fiber 8 or RT4 1001-1111= Reserved	

242	7-4	Module TX media lane 3 wavelength mapping	0000= Mapping unknown or undefined 0001= Maps to module media wavelength 1 0010= Maps to module media wavelength 2 0011= Maps to module media wavelength 3 0100= Maps to module media wavelength 4 0101= Maps to module media wavelength 5 0110= Maps to module media wavelength 6 0111= Maps to module media wavelength 7 1000= Maps to module media wavelength 8 1001-1111= Reserved	RO Opt.
	3-0	Module TX media lane 3 fiber mapping	0000= Mapping unknown or undefined 0001= Maps to module media fiber 1 or TR1 0010= Maps to module media fiber 2 or RT1 0011= Maps to module media fiber 3 or TR2 0100= Maps to module media fiber 4 or RT2 0101= Maps to module media fiber 5 or TR3 0110= Maps to module media fiber 6 or RT3 0111= Maps to module media fiber 7 or TR4 1000= Maps to module media fiber 8 or RT4 1001-1111= Reserved	
243	7-4	Module TX media lane 4 wavelength mapping	0000= Mapping unknown or undefined 0001= Maps to module media wavelength 1 0010= Maps to module media wavelength 2 0011= Maps to module media wavelength 3 0100= Maps to module media wavelength 4 0101= Maps to module media wavelength 5 0110= Maps to module media wavelength 6 0111= Maps to module media wavelength 7 1000= Maps to module media wavelength 8 1001-1111= Reserved	RO Opt.
	3-0	Module TX media lane 4 fiber mapping	0000= Mapping unknown or undefined 0001= Maps to module media fiber 1 or TR1 0010= Maps to module media fiber 2 or RT1 0011= Maps to module media fiber 3 or TR2 0100= Maps to module media fiber 4 or RT2 0101= Maps to module media fiber 5 or TR3 0110= Maps to module media fiber 6 or RT3 0111= Maps to module media fiber 7 or TR4 1000= Maps to module media fiber 8 or RT4 1001-1111= Reserved	
244	7-4	Module TX media lane 5 wavelength mapping	0000= Mapping unknown or undefined 0001= Maps to module media wavelength 1 0010= Maps to module media wavelength 2 0011= Maps to module media wavelength 3 0100= Maps to module media wavelength 4 0101= Maps to module media wavelength 5 0110= Maps to module media wavelength 6 0111= Maps to module media wavelength 7 1000= Maps to module media wavelength 8 1001-1111= Reserved	RO Opt.

	3-0	Module TX media lane 5 fiber mapping	0000= Mapping unknown or undefined 0001= Maps to module media fiber 1 or TR1 0010= Maps to module media fiber 2 or RT1 0011= Maps to module media fiber 3 or TR2 0100= Maps to module media fiber 4 or RT2 0101= Maps to module media fiber 5 or TR3 0110= Maps to module media fiber 6 or RT3 0111= Maps to module media fiber 7 or TR4 1000= Maps to module media fiber 8 or RT4 1001-1111= Reserved	
245	7-4	Module TX media lane 6 wavelength mapping	0000= Mapping unknown or undefined 0001= Maps to module media wavelength 1 0010= Maps to module media wavelength 2 0011= Maps to module media wavelength 3 0100= Maps to module media wavelength 4 0101= Maps to module media wavelength 5 0110= Maps to module media wavelength 6 0111= Maps to module media wavelength 7 1000= Maps to module media wavelength 8 1001-1111= Reserved	RO Opt.
	3-0	Module TX media lane 6 fiber mapping	0000= Mapping unknown or undefined 0001= Maps to module media fiber 1 or TR1 0010= Maps to module media fiber 2 or RT1 0011= Maps to module media fiber 3 or TR2 0100= Maps to module media fiber 4 or RT2 0101= Maps to module media fiber 5 or TR3 0110= Maps to module media fiber 6 or RT3 0111= Maps to module media fiber 7 or TR4 1000= Maps to module media fiber 8 or RT4 1001-1111= Reserved	
246	7-4	Module TX media lane 7 wavelength mapping	0000= Mapping unknown or undefined 0001= Maps to module media wavelength 1 0010= Maps to module media wavelength 2 0011= Maps to module media wavelength 3 0100= Maps to module media wavelength 4 0101= Maps to module media wavelength 5 0110= Maps to module media wavelength 6 0111= Maps to module media wavelength 7 1000= Maps to module media wavelength 8 1001-1111= Reserved	RO Opt.
	3-0	Module TX media lane 7 fiber mapping	0000= Mapping unknown or undefined 0001= Maps to module media fiber 1 or TR1 0010= Maps to module media fiber 2 or RT1 0011= Maps to module media fiber 3 or TR2 0100= Maps to module media fiber 4 or RT2 0101= Maps to module media fiber 5 or TR3 0110= Maps to module media fiber 6 or RT3 0111= Maps to module media fiber 7 or TR4 1000= Maps to module media fiber 8 or RT4 1001-1111= Reserved	

247	7-4	Module TX media lane 8 wavelength mapping	0000= Mapping unknown or undefined 0001= Maps to module media wavelength 1 0010= Maps to module media wavelength 2 0011= Maps to module media wavelength 3 0100= Maps to module media wavelength 4 0101= Maps to module media wavelength 5 0110= Maps to module media wavelength 6 0111= Maps to module media wavelength 7 1000= Maps to module media wavelength 8 1001-1111= Reserved	RO Opt.
	3-0	Module TX media lane 8 fiber mapping	0000= Mapping unknown or undefined 0001= Maps to module media fiber 1 or TR1 0010= Maps to module media fiber 2 or RT1 0011= Maps to module media fiber 3 or TR2 0100= Maps to module media fiber 4 or RT2 0101= Maps to module media fiber 5 or TR3 0110= Maps to module media fiber 6 or RT3 0111= Maps to module media fiber 7 or TR4 1000= Maps to module media fiber 8 or RT4 1001-1111= Reserved	
248	7-4	Module RX media lane 1 wavelength mapping	0000= Mapping unknown or undefined 0001= Maps to module media wavelength 1 0010= Maps to module media wavelength 2 0011= Maps to module media wavelength 3 0100= Maps to module media wavelength 4 0101= Maps to module media wavelength 5 0110= Maps to module media wavelength 6 0111= Maps to module media wavelength 7 1000= Maps to module media wavelength 8 1001-1111= Reserved	RO Opt.
	3-0	Module RX media lane 1 fiber mapping	0000= Mapping unknown or undefined 0001= Maps to module media fiber 1 or RT1 0010= Maps to module media fiber 2 or TR1 0011= Maps to module media fiber 3 or RT2 0100= Maps to module media fiber 4 or TR2 0101= Maps to module media fiber 5 or RT3 0110= Maps to module media fiber 6 or TR3 0111= Maps to module media fiber 7 or RT4 1000= Maps to module media fiber 8 or TR4 1001-1111= Reserved	
249	7-4	Module RX media lane 2 wavelength mapping	0000= Mapping unknown or undefined 0001= Maps to module media wavelength 1 0010= Maps to module media wavelength 2 0011= Maps to module media wavelength 3 0100= Maps to module media wavelength 4 0101= Maps to module media wavelength 5 0110= Maps to module media wavelength 6 0111= Maps to module media wavelength 7 1000= Maps to module media wavelength 8 1001-1111= Reserved	RO Opt.

	3-0	Module RX media lane 2 fiber mapping	0000= Mapping unknown or undefined 0001= Maps to module media fiber 1 or RT1 0010= Maps to module media fiber 2 or TR1 0011= Maps to module media fiber 3 or RT2 0100= Maps to module media fiber 4 or TR2 0101= Maps to module media fiber 5 or RT3 0110= Maps to module media fiber 6 or TR3 0111= Maps to module media fiber 7 or RT4 1000= Maps to module media fiber 8 or TR4 1001-1111= Reserved	
250	7-4	Module RX media lane 3 wavelength mapping	0000= Mapping unknown or undefined 0001= Maps to module media wavelength 1 0010= Maps to module media wavelength 2 0011= Maps to module media wavelength 3 0100= Maps to module media wavelength 4 0101= Maps to module media wavelength 5 0110= Maps to module media wavelength 6 0111= Maps to module media wavelength 7 1000= Maps to module media wavelength 8 1001-1111= Reserved	RO Opt.
	3-0	Module RX media lane 3 fiber mapping	0000= Mapping unknown or undefined 0001= Maps to module media fiber 1 or RT1 0010= Maps to module media fiber 2 or TR1 0011= Maps to module media fiber 3 or RT2 0100= Maps to module media fiber 4 or TR2 0101= Maps to module media fiber 5 or RT3 0110= Maps to module media fiber 6 or TR3 0111= Maps to module media fiber 7 or RT4 1000= Maps to module media fiber 8 or TR4 1001-1111= Reserved	
251	7-4	Module RX media lane 4 wavelength mapping	0000= Mapping unknown or undefined 0001= Maps to module media wavelength 1 0010= Maps to module media wavelength 2 0011= Maps to module media wavelength 3 0100= Maps to module media wavelength 4 0101= Maps to module media wavelength 5 0110= Maps to module media wavelength 6 0111= Maps to module media wavelength 7 1000= Maps to module media wavelength 8 1001-1111= Reserved	RO Opt.
	3-0	Module RX media lane 4 fiber mapping	0000= Mapping unknown or undefined 0001= Maps to module media fiber 1 or RT1 0010= Maps to module media fiber 2 or TR1 0011= Maps to module media fiber 3 or RT2 0100= Maps to module media fiber 4 or TR2 0101= Maps to module media fiber 5 or RT3 0110= Maps to module media fiber 6 or TR3 0111= Maps to module media fiber 7 or RT4 1000= Maps to module media fiber 8 or TR4 1001-1111= Reserved	

252	7-4	Module RX media lane 5 wavelength mapping	0000= Mapping unknown or undefined 0001= Maps to module media wavelength 1 0010= Maps to module media wavelength 2 0011= Maps to module media wavelength 3 0100= Maps to module media wavelength 4 0101= Maps to module media wavelength 5 0110= Maps to module media wavelength 6 0111= Maps to module media wavelength 7 1000= Maps to module media wavelength 8 1001-1111= Reserved	RO Opt.
	3-0	Module RX media lane 5 fiber mapping	0000= Mapping unknown or undefined 0001= Maps to module media fiber 1 or RT1 0010= Maps to module media fiber 2 or TR1 0011= Maps to module media fiber 3 or RT2 0100= Maps to module media fiber 4 or TR2 0101= Maps to module media fiber 5 or RT3 0110= Maps to module media fiber 6 or TR3 0111= Maps to module media fiber 7 or RT4 1000= Maps to module media fiber 8 or TR4 1001-1111= Reserved	
253	7-4	Module RX media lane 6 wavelength mapping	0000= Mapping unknown or undefined 0001= Maps to module media wavelength 1 0010= Maps to module media wavelength 2 0011= Maps to module media wavelength 3 0100= Maps to module media wavelength 4 0101= Maps to module media wavelength 5 0110= Maps to module media wavelength 6 0111= Maps to module media wavelength 7 1000= Maps to module media wavelength 8 1001-1111= Reserved	RO Opt.
		Module RX media lane 6 fiber mapping	0000= Mapping unknown or undefined 0001= Maps to module media fiber 1 or RT1 0010= Maps to module media fiber 2 or TR1 0011= Maps to module media fiber 3 or RT2 0100= Maps to module media fiber 4 or TR2 0101= Maps to module media fiber 5 or RT3 0110= Maps to module media fiber 6 or TR3 0111= Maps to module media fiber 7 or RT4 1000= Maps to module media fiber 8 or TR4 1001-1111= Reserved	
254		Module RX media lane 7 wavelength mapping	0000= Mapping unknown or undefined 0001= Maps to module media wavelength 1 0010= Maps to module media wavelength 2 0011= Maps to module media wavelength 3 0100= Maps to module media wavelength 4 0101= Maps to module media wavelength 5 0110= Maps to module media wavelength 6 0111= Maps to module media wavelength 7 1000= Maps to module media wavelength 8 1001-1111= Reserved	RO Opt.

		Module RX media lane 7 fiber mapping	0000= Mapping unknown or undefined 0001= Maps to module media fiber 1 or RT1 0010= Maps to module media fiber 2 or TR1 0011= Maps to module media fiber 3 or RT2 0100= Maps to module media fiber 4 or TR2 0101= Maps to module media fiber 5 or RT3 0110= Maps to module media fiber 6 or TR3 0111= Maps to module media fiber 7 or RT4 1000= Maps to module media fiber 8 or TR4 1001-1111= Reserved	
255	7-4	Module RX media lane 8 wavelength mapping	0000= Mapping unknown or undefined 0001= Maps to module media wavelength 1 0010= Maps to module media wavelength 2 0011= Maps to module media wavelength 3 0100= Maps to module media wavelength 4 0101= Maps to module media wavelength 5 0110= Maps to module media wavelength 6 0111= Maps to module media wavelength 7 1000= Maps to module media wavelength 8 1001-1111= Reserved	RO Opt.
	3-0	Module RX media lane 8 fiber mapping	0000= Mapping unknown or undefined 0001= Maps to module media fiber 1 or RT1 0010= Maps to module media fiber 2 or TR1 0011= Maps to module media fiber 3 or RT2 0100= Maps to module media fiber 4 or TR2 0101= Maps to module media fiber 5 or RT3 0110= Maps to module media fiber 6 or TR3 0111= Maps to module media fiber 7 or RT4 1000= Maps to module media fiber 8 or TR4 1001-1111= Reserved	

2 Appendix A – Form Factor Signal Names

Table 81 associates form factor-specific terminology and signal names for three form factors with the generic terms used in this specification.

Table 77- Form Factor Signal Name Associations

CMIS generic name	**QSFP-DD**	**OSFP**	**COBO**
Reset signal	ResetL	RSTn	ResetL
Interrupt signal	IntL	INT	IntL
Init mode signal		uses LPWn pin to select SW or HW power up processes.	
Hardware Init mode	InitMode = 0		InitMode=0
Software Init mode	InitMode = 1		InitMode=1
LowPwr signal	N/A	LPWn	N/A

3 Appendix B – Host-Module Initialization Example Flows

This appendix includes some example flows that illustrate interactions between the host and module during module initialization. Refer to Section 1.4 for Module State Machine details and Section 1.5 for Data Path State Machine, Application, and Control Set details.

3.1 Software Init Mode (INITMODE=1) Default

The following table provides an example of a simple module power-up sequence where the module powers up under host software control (InitMode=1) and with the following key attributes:

1. Module is powered-up from an un-powered state
2. Module is powered-up under host software control (InitMode=1)
3. Host selects one of the advertised Applications advertised by the module.
4. Host uses the default settings for the selected Application. The host does not use custom signal integrity settings (i.e. Explicit Control indicator)
5. Host uses only staged Control Set 0 to configure the module (optional Staged Control Set 1 is not used).
6. No speed negotiation

#		Host Action		Module Action		Module State (M) Data Path State (D)
0		Host turns off Vcc, InitMode=1, ResetL=1		Module electronics held in reset		M=NA D=NA
1		Hot Plug				
2		Host detects ModPrsL	<-			
3		Host applies Vcc				
4		Host de-asserts ResetL	->			
5		Host waits for IntL or 2 s		Module powers up and initializes the management interface See Section 1.4.4.		M=MgntInit D=DataPathDeactivated
6				When management initialization is complete the module enters ModuleLowPwr state, sets the Module State Changed interrupt flag (See Section 1.7.2.3) and asserts IntL signal.		M=ModuleLowPwr D=DataPathDeactivated
7		Host acknowledges the module state change by reading latch interrupt registers which clears IntL See Table 21 (Page 00h, Register 8).	<-	Module waits for host action		
8		Host reads module information (See 1.7.2.2 through 1.7.2.7) including advertised Applications (See Table 26)				
9		Host reads timeouts for ModulePwrUp, ModulePwrDn, DataPathInit and DataPathDeinit states (See Table 40)				

#	Host Action		Module Action	Module State (M) Data Path State (D)
10	Host selects the Applications (and associated host electrical lane mappings) it wants to configure by writing into the Staged Control Set 0 Application Select Control registers (See Table 56), with the associated Explicit Control bits set to 0 (i.e. use Application defined settings).			
11	Host asserts Apply_DataPathInit bits for all associated host lanes of the selected Application to copy Staged Control Set 0 to the Active Control Set See Table 55, (Page 10h, Register 143).	->		
12			Module validates the configuration requested in Staged Control Set 0. If the configuration was found to be valid, the module copies the contents to the Active Control Set. If the configuration was found to be invalid the module sets the appropriate lane bytes in the Configuration Error Code fields.	
13	Host reads the Configuration Error Code fields (See Table 71 and Table 72) to confirm that the requested configuration was verified and accepted by the module for all associated lanes of the selected Application.	<-		
14	Host asserts Tx Disable (See Table 54) for all media lanes for Applications being configured (to ensure each Application is initialized with associated optical output lanes disabled to avoid link flapping).			

#	Host Action		Module Action	Module State (M) Data Path State (D)
15	Host configures other lane specific controls by writing to Lane Specific Control Field registers (See Table 54).			
16	When a host wants to enable one of the data paths(Applications) that it has pre-configured, it first configures the line card port to be consistent with the Application and it then enables the associated Tx electrical output lanes to the module. This is required to ensure that when the module is subsequently powering up the requested data path that it has valid data on it’s TX electrical input lanes			
17	Host sets the DataPathPwrUp bits for all host lanes in the data path(s) that it wants to enable (See Table 53, Page 10h Register 128).	->		
18			Module sets the Module state register to ModulePwrUp (See Table 18 and Table 19) and the Data Path state register to DataPathInit (See Table 65), to indicate that it is taking control from the host and beginning to power up the requested data path(s).	M=ModulePwrUp D=DataPathInit
19			Module powers up the data path(s) as described in Section 1.5.3.2.	
20			When the requested data paths are powered up the Module enters the ModuleReady and DataPathActivated states by updating the associated state registers (See Table 18 Table 19 and Table 65) and asserts the IntL signal.	M=ModuleReady D=DataPathActivated
		<-		

#	Host Action	Module Action	Module State (M) Data Path State (D)
21	Host acknowledges the module state change by reading latch interrupt registers which clears IntL (See Table 21, Page 00h, Register 8).		
22	Host de-asserts Tx Disable (See Table 51) for all media lanes of the data path(s) that it wants to enable the Tx optical outputs on.		

3.2 Module power-down sequence example

The following table provides an example of a simple module power-down sequence using host software control (InitMode=1), where the starting point is with the module powered-up and at least one data path in the DataPathActivated state.

#	Host Action		Module Action	Module State (M) Data Path State (D)
0	Module is powered up with at least one data path activated.			M=ModuleReady D=DataPathActivated
1	The host clears the DataPathPwrUp bit for all host lanes in the applicable data path (See Table 53, Page 10h Register 128).	->		
2			Module sets the Data Path state register to DataPathDeInit (See Table 65), to indicate that it is taking control from the host and begins to de-initialize the requested data path as decribed in Section 1.5.3.4. The module also disables the Tx media output lanes on the associated data path.	M=ModuleReady D=DataPathDeinit

#	Host Action		Module Action	Module State (M) Data Path State (D)
3			When the requested data path is de-initalized the module enters the DataPathDeActivated state by updating the associated Data Path state registers (See Table 65) and asserts the IntL signal. Note the same data path state code is reported in the Data Path state registers for all host lanes of the associated data path (although the host may determine the data path state by reading the data path state code from only one of the host lane registers in the data path).	M=ModuleReady D=DataPathDeActivated
		<-		
4	Host acknowledges the Data Path state change by reading latched module flag registers which clears IntL (See Table 21, Page 00h Register 8).			
5	If the Host wishes to fully power down the module, the Host sets the ForceLowPwr bit (See Table 23, Page 00h Register 26).	->		
6			Module sets Module state register to ModulePwrDn (See Table 65) to inform the host that the module is in the process of returning to Low Power mode. The module shall also transition all Data Path States to DataPathDeinit.	M=ModulePwrDn D=DataPathDeActivated

#	Host Action		Module Action	Module State (M) Data Path State (D)
7			When all the data paths reach the DataPathDeactivated state and the module is in low power mode, the module shall 1)transition to the ModuleLowPwr state, 2)transition all data paths that are in DataPathInit or DataPathActivated to DataPathDeinit 3)update the associated Module and Data Path state registers (See Table 18, Table 19 and Table 65) 4)assert the IntL signal.	M=ModuleLowPwr D=DataPathDeActivated
8	Host acknowledges the Module and Data Path state change by reading latched module flag registers which clears IntL (See Table 21, Page 00h Register 8).	<-		

4 Appendix C – Media advertising codes

This section provides the advertising codes for both host electrical and module media interfaces. The codes for applications supported by the module are entered by the module into the Module Host-Media Interfaces advertising registers shown in Table 26 and Table 48. The host selects the advertised (ApSel) code for the desired supported application and enters it into the application select registers shown in Table 56 (section 1.7.6.3) and Table 60 (section 1.7.6.4). Table 25 (Page 00h byte 85) identifies which of the media interface code tables (Table 79 - Table 83) applies to the module. Table 79 - Table 83 are independent of Table 36 where media interface technology is listed.

Table 78- Module Host Electrical Interfaces Codes

ID	Code (Hex)	Application Name	Application Data Rate, Gb/s	Lane Count	Lane Signal Rate, GBd	Modulation	b/sym
0	0	Undefined					
		Ethernet Applications					
1	1	1000BASE -CX (Clause 39)	1.25	1	1.25	NRZ	1
2	2	XAUI (Clause 47)	12.50	4	3.125	NRZ	1
3	3	XFI (SFF INF-8071i)	9.95-11.18	1	9.95-11.18	NRZ	1
4	4	SFI (SFF-8431)	9.95-11.18	1	9.95-11.18	NRZ	1
5	5	25GAUI C2M (Annex 109B)	25.78	1	25.78125	NRZ	1
6	6	XLAUI C2M (Annex 83B)	41.25	4	10.3125	NRZ	1
7	7	XLPPI (Annex 86A)	41.25	4	10.3125	NRZ	1
8	8	LAUI-2 C2M (Annex 135C)	51.56	2	25.78125	NRZ	1
9	9	50GAUI-2 C2M (Annex 135E)	53.13	2	26.5625	NRZ	1
10	A	50GAUI-1 C2M (Annex 135G)	53.13	1	26.5625	PAM4	2
11	B	CAUI-4 C2M (Annex 83E)	103.13	4	25.78125	NRZ	1
12	C	100GAUI-4 C2M (Annex 135E)	106.25	4	26.5625	NRZ	1
13	D	100GAUI-2 C2M (Annex 135G)	106.25	2	26.5625	PAM4	2
14	E	200GAUI-8 C2M (Annex 120C)	212.50	8	26.5625	NRZ	1
15	F	200GAUI-4 C2M (Annex 120E)	212.50	4	26.5625	PAM4	2
16	10	400GAUI-16 C2M (Annex 120C)	425.00	16	26.5625	NRZ	1
17	11	400GAUI-8 C2M (Annex 120E)	425.00	8	26.5625	PAM4	2
18	12	Reserved					
19	13	10GBASE-CX4 (Clause 54)	12.50	4	3.125	NRZ	1
20	14	25GBASE-CR CA-L (Clause 110)	25.78	1	25.78125	NRZ	1
21	15	25GBASE-CR CA-S (Clause 110)	25.78	1	25.78125	NRZ	1
22	16	25GBASE-CR CA-N (Clause 110)	25.78	1	25.78125	NRZ	1
23	17	40GBASE-CR4 (Clause 85)	41.25	4	10.3125	NRZ	1
24	18	50GBASE-CR (Clause 126)	53.13	1	26.5625	PAM4	2
25	19	100GBASE-CR10 (Clause 85)	103.13	10	10.3125	NRZ	1
26	1A	100GBASE-CR4 (Clause 92)	103.13	4	25.78125	NRZ	1

27	1B	100GBASE-CR2 (Clause 136)	106.25	2	26.5625	PAM4	2
28	1C	200GBASE-CR4 (Clause 136)	212.50	4	26.5625	PAM4	2
29	1D	400G CR8 ()	425.00	8	26.5625	PAM4	2
30	1E	1000BASE -T (Clause 40)	1.12	4	0.125	PAM5	2.236 068
31	1F	2.5GBASE-T (Clause 126)	2.50	4	0.200	PAM16	3.125
32	20	5GBASE-T (Clause 126)	5.00	4	0.400	PAM16	3.125
33	21	10GBASE-T (Clause 55)	10.00	4	0.800	PAM16	3.125
34	22	25GBASE-T (Clause 113)	25	4	2.000	PAM16	3.125
35	23	40GBASE-T (Clause 113)	40	4	3.200	PAM16	3.125
36	24	50GBASE-T ()					
		Fibre Channel Applications					
37	25	8GFC (FC-PI -4)	8.50	1	8.500	NRZ	1
38	26	10GFC (10GFC)	10.52	1	10.51875	NRZ	1
39	27	16GFC (FC-PI -5)	14.03	1	14.025	NRZ	1
40	28	32GFC (FC-PI -6)	28.05	1	28.050	NRZ	1
41	29	64GFC (FC-PI -7)	57.80	1	28.900	PAM4	2
42	2A	128GFC (FC-PI -6P)	112.20	4	28.050	NRZ	1
43	2B	256GFC (FC-PI -7P)	231.20	4	28.900	PAM4	2
		InfiniBand Applications					
44	2C	IB SDR (Arch.Spec.Vol.2 R.1.3.1)	2.5 - 30	1, 2, 4, 8, 12	2.5	NRZ	1
45	2D	IB DDR (Arch.Spec.Vol.2 R.1.3.1)	5.0 - 60	1, 2, 4, 8, 12	5.0	NRZ	1
46	2E	IB QDR (Arch.Spec.Vol.2 R.1.3.1)	10 - 120	1, 2, 4, 8, 12	10.0	NRZ	1
47	2F	IB FDR (Arch.Spec.Vol.2 R.1.3.1)	14 - 169	1, 2, 4, 8, 12	14.0625	NRZ	1
48	30	IB EDR (Arch.Spec.Vol.2 R.1.3.1)	26 - 309	1, 2, 4, 8, 12	25.78125	NRZ	1
49	31	IB HDR (Arch.Spec.Vol.2 R.1.3.1)	52 - 618	1, 2, 4, 8, 12	26.5625	PAM4	2
50	32	IB NDR	Nx100G				
		CIPRI Applications					
51	33	E.96 (CPRI Specification V7.0)	9.83	1	9.8304	NRZ	1
52	34	E.99 (CPRI Specification V7.0)	10.14	1	10.1376	NRZ	1
53	35	E.119 (CPRI Specification V7.0)	12.17	1	12.16512	NRZ	1
54	36	E.238 (CPRI Specification V7.0)	24.33	1	24.33024	NRZ	1

		OTN Applications					
55	37	OTL3.4 (ITU-T G.709/Y.1331 G.Sup58) See XLAUI (overclocked)	43	4	10.7546	NRZ	1
56	38	OTL4.10 (ITU-T G.709/Y.1331 G.Sup58) See CAUI-10 (overclocked)	112	10	11.1810	NRZ	1
57	39	OTL4.4 (ITU-T G.709/Y.1331 G.Sup58)See CEI-28G-VSR	112	4	27.9525	NRZ	1
58	3A	OTLC.4 (ITU-T G.709/Y.1331 G.Sup58) See CEI-28G-VSR	112	4	28.0762	NRZ	1
59	3B	FOIC1.4 (ITU-T G.709/Y.1331 G.Sup58) See CEI-28G-VSR	112	4	27.9524	NRZ	1
60	3C	FOIC1.2 (ITU-T G.709/Y.1331 G.Sup58) See CEI-56G-VSR-PAM4	112	2	27.9524	PAM4	2
61	3D	FOIC2.8 (ITU-T G.709/Y.1331 G.Sup58	224	8	27.9523	NRZ	1
62	3E	FOIC2.8 (ITU-T G.709/Y.1331 G.Sup58	224	4	27.9523	PAM4	2
63	3F	FOIC2.8 (ITU-T G.709/Y.1331 G.Sup58	447	16	27.9523	NRZ	1
64	40	FOIC2.8 (ITU-T G.709/Y.1331 G.Sup58	447	8	27.9523	PAM4	2
61: 191	3D:BF	Reserved					
192: 254	C0:FE	Custom					
255	FF	End of list					

Table 79- 850 nm MM media interface advertising codes

ID	**Code (Hex)**	**Application Name**	**Application Data Rate, Gb/s**	**Lane Count**	**Lane Signal Rate, GBd**	**Modulation**	**b/sym**
0	0	Undefined					
		Ethernet Applications					
1	1	10GBASE-SW (Clause 52)	9.95	1	9.95328	NRZ	1
2	2	10GBASE-SR (Clause 52)	10.31	1	10.3125	NRZ	1
3	3	25GBASE-SR (Clause 112)	25.78	1	25.78125	NRZ	1
4	4	40GBASE-SR4 (Clause 86)	41.25	4	10.3125	NRZ	1
5	5	40GE SWDM4 MSA Spec	41.25	4	10.3125	NRZ	1
6	6	40GE BiDi	41.25	2	20.625	NRZ	1
7	7	50GBASE-SR (Clause 138)	53.13	1	26.5625	PAM4	2
8	8	100GBASE-SR10 (Clause 86)	103.13	10	10.3125	NRZ	1
9	9	100GBASE-SR4 (Clause 95)	103.13	4	25.78125	NRZ	1
10	A	100GE SWDM4 MSA Spec	103.13	4	25.78125	NRZ	1
11	B	100GE BiDi	106.25	2	25.5625	PAM4	2

12	C	100GBASE-SR2 (Clause 138)	106.25	2	26.5625	PAM4	2
13	D	100G-SR					
14	E	200GBASE-SR4 (Clause 138)	212.50	4	26.5625	PAM4	2
15	F	400GBASE-SR16 (Clause 123)	425.00	16	26.5625	NRZ	1
16	10	400G-SR8					
17	11	400G-SR4					
18	12	800G-SR8					
26	1A	400GE BiDI	425.00	8	26.5625	PAM4	2
		Fibre Channel Applications					
19	13	8GFC-MM (FC-PI -4)	8.50	1	8.500	NRZ	1
20	14	10GFC-MM (10GFC)	10.52	1	10.51875	NRZ	1
21	15	16GFC-MM (FC-PI -5)	14.03	1	14.025	NRZ	1
22	16	32GFC-MM (FC-PI -6)	28.05	1	28.050	NRZ	1
23	17	64GFC-MM (FC-PI -7)	57.80	1	28.900	PAM4	2
24	18	128GFC-MM4 (FC-PI -6P)	112.20	4	28.050	NRZ	1
25	19	256GFC-MM4 (FC-PI -7P)	231.20	4	28.900	PAM4	2
27: 191	1B:BF	Reserved					
192: 255	C0:FF	Custom					

Table 80- SM media interface advertising codes

ID	**Code (Hex)**	**Application Name**	**Application Data Rate, Gb/s**	**Lane Count**	**Lane Signal Rate, GBd**	**Modulation**	**b/sym**
0	0	Undefined					
		Ethernet Applications					
1	1	10GBASE-LW (Cl 52)	9.95	1	9.953	NRZ	1
2	2	10GBASE-EW (Cl 52)	9.95	1	9.953	NRZ	1
3	3	10G-ZW	9.95	1	9.953	NRZ	1
4	4	10GBASE-LR (Cl 52)	10.31	1	10.3125	NRZ	1
5	5	10GBASE-ER (Cl 52)	10.31	1	10.3125	NRZ	1
6	6	10G-ZR	10.31	1	10.3125	NRZ	1
7	7	25GBASE-LR (Cl 114)	25.78	1	25.78125	NRZ	1
8	8	25GBASE-ER (Cl 114)	25.78	1	25.78125	NRZ	1
9	9	40GBASE-LR4 (Cl 87)	41.25	4	10.3125	NRZ	1
10	A	40GBASE-FR (Cl 89)	41.25	1	41.25	NRZ	1
11	B	50GBASE-FR (Cl 139)	53.13	1	26.5625	PAM4	2
12	C	50GBASE-LR (Cl 139)	53.13	1	26.5625	PAM4	2
13	D	100GBASE-LR4 (Cl 88)	103.13	4	25.78125	NRZ	1
14	E	100GBASE-ER4 (Cl 88)	103.13	4	25.78125	NRZ	1
15	F	100G PSM4 MSA Spec	103.13	4	25.78125	NRZ	1

52	34	100G CWDM4-OCP	103.13	4	25.78125	NRZ	1
16	10	100G CWDM4 MSA Spec	103.13	4	25.78125	NRZ	1
17	11	100G 4WDM-10 MSA Spec	103.13	4	25.78125	NRZ	1
18	12	100G 4WDM-20 MSA Spec	103.13	4	25.78125	NRZ	1
19	13	100G 4WDM-40 MSA Spec	103.13	4	25.78125	NRZ	1
20	14	100GBASE-DR (Cl 140)	106.25	1	53.125	PAM4	2
21	15	100G-FR					
22	16	100G-LR					
23	17	200GBASE-DR4 (Cl 121)	212.50	4	26.5625	PAM4	2
24	18	200GBASE-FR4 (Cl 122)	212.50	4	26.5625	PAM4	2
25	19	200GBASE-LR4 (Cl 122)	212.50	4	26.5625	PAM4	2
26	1A	400GBASE-FR8 (Cl 122)	425.00	8	26.5625	PAM4	2
27	1B	400GBASE-LR8 (Cl 122)	425.00	8	26.5625	PAM4	2
28	1C	400GBASE-DR4 (Cl 124)	425.00	4	53.125	PAM4	2
29	1D	400G-FR4					
30	1E	400G-LR4					
		Fibre Channel Applications					
31	1F	8GFC-SM (FC-PI -4)	8.50	1	8.500	NRZ	1
32	20	10GFC-SM (10GFC)	10.52	1	10.51875	NRZ	1
33	21	16GFC-SM (FC-PI-5)	14.03	1	14.025	NRZ	1
34	22	32GFC-SM (FC-PI-6)	28.05	1	28.050	NRZ	1
35	23	64GFC-SM (FC-PI-7)	57.80	1	28.900	PAM4	2
36	24	128GFC-PSM4 (FC-PI-6P)	112.20	4	28.050	NRZ	1
37	25	256GFC-PSM4 (FC-PI-7P)	231.20	4	28.900	PAM4	2
38	26	128GFC-CWDM4 (FC-PI-6P)	112.20	4	28.050	NRZ	1
39	27	256GFC-CWDM4 (FC-PI-7P)	231.20	4	28.900	PAM4	2
40-43	28-2B	Reserved					
		OTN Applications					
44	2C	4I1-9D1F	112	4	28	NRZ	1
45	2D	4L1-9C1F	112	4	28	NRZ	1
46	2E	4L1-9D1F	112	4	28	NRZ	1
47	2F	C4S1-9D1F	112	4	28	NRZ	1
48	30	C4S1-4D1F	224	4	27.9523	PAM4	2
49	31	4I1-4D1F	224	4	27.9523	PAM4	2
50	32	8R1-4D1F	447	8	27.9523	PAM4	2
51	33	8I1-4D1F	447	8	27.9523	PAM4	2
52-55	34-37	Reserved					
		CPRI Applications					
56	38	10G-SR	9.8304	1	9.8304	NRZ	1
57	39	10G-LR	9.8304	1	9.8304	NRZ	1

58	3A	25G-SR	24.33024	1	24.33024	NRZ	1
59	3B	25G-LR	24.33024	1	24.33024	NRZ	1
60	3C	10G-LR-BiDi	9.8304	1	9.8304	NRZ	1
61	3D	25G-LR-BiDi	24.33024	1	24.33024	NRZ	1
62: 191	3E:BF	Reserved					
192: 255	C0:FF	Custom					

Table 81- Passive Copper Cable interface advertising codes

ID	Code (Hex)	Application Name
0	0	Undefined
1	1	Copper cable, see Page 00h Bytes 202 - 208 for description
2:191	2:BF	Reserved
192:255	C0:FF	Custom

Note: Details for the cable assembly interface are defined using the host electrical codes in Table 78.

Table 82- Active Cable assembly media interface advertising codes

ID	Code (Hex)	Application Name
0	0	Undefined
1	1	Active Cable assembly with BER < 10^-12
2	2	Active Cable assembly with BER < 5x10^-5
3	3	Active Cable assembly with BER < 2.4x10^-4
4:191	4:BF	Reserved
192:255	C0:FF	Custom

Note: Details for the cable assembly interface are defined using the host electrical codes in Table 78.

Table 83- Base-T media interface advertising codes

ID	Code (Hex)	Application Name	Application Data Rate, Gb/s	Lane Count	Lane Signal Rate, GBd	Modulation	
0	0	Undefined					
		Ethernet Applications					
1	1	1000BASE -T (Clause 40)	1.12	4	0.125	PAM5	2.236068
2	2	2.5GBASE-T (Clause 126)	2.50	4	0.200	PAM16	3.125
3	3	5GBASE-T (Clause	5.00	4	0.400	PAM16	3.125

		126)					
4	4	10GBASE-T (Clause 55)	10.00	4	0.800	PAM16	3.125
5:191	5:BF	Reserved					
192:255	C0:FF	Custom					

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