QSFP-DD MSA

QSFP-DD Hardware Specification

for

QSFP DOUBLE DENSITY 8X PLUGGABLE TRANSCEIVER

Revision 5.1

August 7, 2020

Abstract: This specification defines: the electrical and optical connectors, electrical signals and power supplies, mechanical and thermal requirements of the pluggable QSFP Double Density (QSFP-DD) module, connector and cage system. This document provides a common specification for systems manufacturers, system integrators, and suppliers of modules.

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Dedication:
The members of the QSFP-DD MSA would like to acknowledge the contributions of Mr. Edmund Poh. He was an excellent engineer; his technical skills and collaborative attitude will be missed.

The following are Promoter member companies of the QSFP-DD MSA.

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Change History:

Revision	Date	Changes
1.0	Sept 19, 2016	First public release
2.0	March 13, 2017	Second public release
3.0	Sept 19 2017	Third public release
4.0	Sept 18, 2018	Fourth public release, Additions to thermal chapter 6, synchronous clocking in 4.4, Mechanical updates.
5.0	July 9, 2019	Fifth public release, Added Module type 2A, module label drawings, changes to latch drawings, added ePPS pin, updated power supply testing, added BiDi optical port assignments, updated cage drawings.
5.1	August 7, 2020	Chapter 7-Management Interface is now part of Chapter 4-Electrical Specification. Port mapping, optical connectors, and module color coding moved out of Mechanical and Board Definition Chapter-5 and into a new Chapter-5.

Foreword

The development work on this specification was done by the QSFP-DD MSA, an industry group. The membership of the committee since its formation on Feb 2016 has included a mix of companies which are leaders across the industry.

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1 Scope

The scope of this specification is the definition of a high density 8-channel (8x) module, cage and connector system. QSFP-DD supports up to 400 Gb/s in aggregate over an 8 x 50 Gb/s electrical interface. The cage and connector design provides backwards compatibility to QSFP28 modules which can be inserted into a QSFP-DD port and connected to 4 of the 8 electrical channels.

This specification is intended to be used in combination with the Common Management Interface Specification (CMIS). Mutual dependencies exist for timing parameters, management interface and register specifications.

1.1 Description of Chapters

QSFP-DD specifications is organized in to 7 chapters and 3 appendixes addressing electrical/management, optical, mechanical, and environmental aspect of the module.

- Chapter 1 Scope and Purpose
- Chapter 2 Reference and Related Standards and SFF Specifications
- Chapter 3 Introduction
- Chapter 4 Electrical Specifications and Management Interface Timing
- Chapter 5 Optical Port Mapping and Optical Interfaces
- Chapter 6 Mechanical specifications and printed circuit board recommendations
- Chapter 7 Environmental and thermal considerations.
- Appendix A Informative overall module length with elastomeric handle
- Appendix B Informative Module Type 2A Heatsink Examples Informative Module Type 2A Heat Sink Examples
- Appendix C Normative Module and Connector performance requirements.

2 References

2.1 Industry Documents

The following documents are relevant to this Specification:
- ANSI FC-PI-6 32GFC
- ANSI FC-PI-7 64GFC
- ASME Y14.5-2009 Dimensioning and Tolerancing
- Common Management Interface Specification (CMIS) 4.0
- CS-01242017 CS optical connector and receptacle, see http://www.qsfp-dd.com/optical-connector/
- EN6100-4-2 (IEC immunity standard on ESD), criterion B test specification
- Human Body Model per ANSI/ESDA/JEDEC JS-001
- IEC/UL 60950-1 Requirements for Information Technology Equipment, Section 4.5.4 (Touch Temperature Reference)
- IEC 61754-7-1 (Fibre Optic Interconnecting Devices and Passive Components - Fibre Optic Connector
- IEEE Std 802.3™-2018
- IEEE Std 802.3cd (50 Gb/s, 100 Gb/s, and 200 Gb/s Ethernet)
- IEEE Std 802.3ck (100 Gb/s, 200 Gb/s, and 400 Gb/s Electrical Interfaces)
- IEEE Std 802.3cm-2020 clause 150-BiDi (Physical Layer and Management Parameters for 400 Gb/s over Multimode Fiber)
- IEEE Std 1588 Precision Clock Synchronization Protocol PTP, 2019
- InfiniBand Architecture Specifications (informative document)
- JEDEC JESD8C.01 Interface Standard for Nominal 3.0/3.3 V Supply Digital Integrated Circuit (LVCMOS)
- Keysight Application Brief 5991-2778EN: Methods for characterizing and tuning DC inrush current (informative document)
- NXP UM10204, I^2C-bus specification and user manual, Rev 6 – 4 April 2014.
- OIF CEI-28G-VSR
- OIF CEI-56G-VSR-PAM4
- SN-60092019 SN optical connector and receptacle, see http://www.qsfp-dd.com/optical-connector/
- Telcordia GR63 NEBSTM Requirements: Physical Protection, Section 4.1.7, December 2017
- TIA-604-5 (FOCIS 5 Fiber Optic Connector Intermateability Standard- Type MPO
- TIA-604-10 (FOCIS 10 Fiber Optic Connector Intermateability Standard- Type LC)
- TIA-604-18 (FOCIS 18 Fiber Optic Connector Intermateability Standard- Type MPO-16

Interfaces - Part 7-1: Type MPO Connector Family - One Fibre Row)
- USC-11383001 MDC optical plug and receptacle, see http://www.qsfp-dd.com/optical-connector/

SFF Specifications:
- SFF-8431 SFP+ 10 Gb/s and Low Speed Electrical Interface, Rev. 4.1
- SFF-8436 QSFP+ 10 Gb/s 4X Pluggable Transceiver, Rev. 4.9.
- SFF-8636 Management Interface for Cabled Environments, Rev. 2.10a.
- SFF-8472 Diagnostic Monitoring Interface for Optical Transceivers, Rev. 12.3.
- SFF-8679 QSFP28 4X Base Electrical Specifications, Rev. 1.8.

2.2 Sources

The QSFP-DD MSA Hardware Specification for QSFP DOUBLE DENSITY 8X PLUGGABLE TRANSCEIVER can be obtained via the www.QSFP-DD.com web site.

3 Introduction

This Specification covers the following items:

a) Electrical interfaces including pad assignments for data, control, status and power supplies and host PCB layout requirements.

b) Optical interfaces (including optical receptacles and mating fiber plugs for multimode and single-mode duplex and parallel fiber applications). Breakout cable applications are also specified. Optical signaling specifications are not included in this document but are defined in the applicable industry standards.

c) Mechanical specifications including dimensions and tolerances for the connector, cage and module system. Includes details of the requirements for correct mating of the module and host sides of the connector.

d) Thermal requirements

e) Electrostatic discharge (ESD) requirements by reference to industry standard limits and test methods.

f) Timing requirements for management interface, low speed I/O, soft control and status functions.

This Specification does not cover the following items:

a) Electromagnetic interference (EMI) protection. EMI protection is the responsibility of the implementers of the cages and modules.

b) Memory map definition, which can be found in the 'Common Management Interface Specification for 8x/16x pluggable transceivers' (see www.QSFP-DD.com).

3.1 Objectives

Implementations compliant to electrical signal contact and channel assignments, electrical and power requirements defined in Chapter 4 and optical lane assignments defined in Chapter 5 ensure that the pluggable modules and cable assemblies are functionally interchangeable. Dimensions, mounting and insertion requirements defined in Chapter 6 for the bezel, optical module, cable plug, cage and connector system on a circuit board ensure that these products are mechanically interchangeable.

3.2 Applications

This specification defines a common eight-lanes pluggable module that, e.g., support Ethernet, InfiniBand, and/or Fibre Channel requirements. The QSFP-DD specification is applicable to pluggable modules or direct attach cables based on multimode fiber, single mode fiber or copper wires.
An application reference Model, shown in Figure 1, shows the high-speed data interface between an ASIC and the QSFP-DD module.

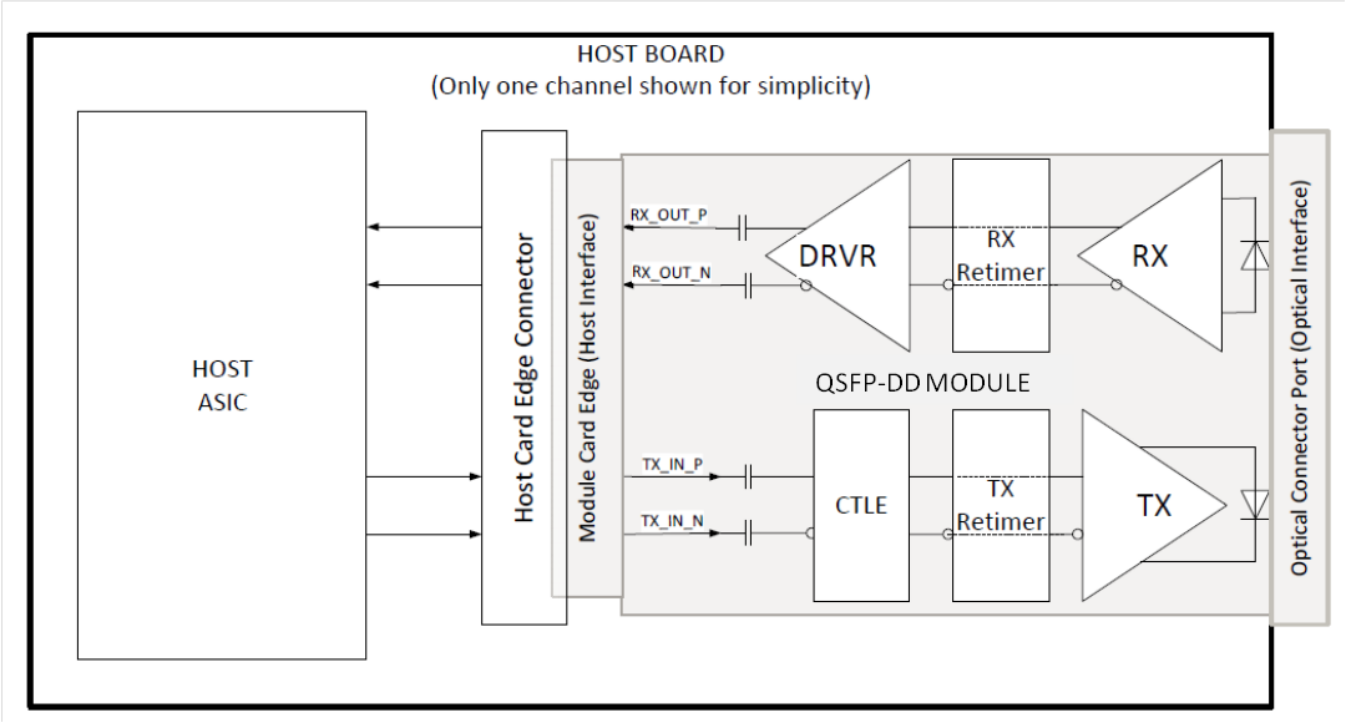


Figure 1: Application Reference Model

Note: For high speed electrical signals the compliance board methodology of IEEE and OIF should be used. Measurements taken with QSFP-DD compliance boards should be corrected for any difference between the loss of these compliance boards and the loss of the compliance boards specified in the standard.

4 Electrical Specification and Management Interface Timing

This Chapter contains signal definitions and requirements that are specific to the QSFP-DD module. High-speed signal requirements including compliance points for electrical measurements are defined in the applicable industry standard.

4.1 Electrical Connector

The QSFP-DD module edge connector consists of a single paddle card with 38 pads on the top and 38 pads on the bottom of the paddle card for a total of 76 pads. The pads are defined in such a manner so as to accommodate insertion of a QSFP+/QSFP28 module into a QSFP-DD receptacle. The legacy signal locations are deeper on the paddlecard, so that legacy QSFP+/QSFP28 module pads only connect to the longer row of connector pins, leaving the short row of connector pins unconnected in a QSFP+/QSFP28 application.

The pads are designed for a sequenced mating:

First mate – ground pads
Second mate – power pads
Third mate – signal pads

Because the QSFP-DD module has 2 rows of pads, the additional QSFP-DD pads will have an intermittent connection with the legacy QSFP+/QSFP28 pins in the connector during the module insertion and removal. The 'legacy' QSFP+ pads have a 'B' label shown in Table 1 to designate them as the second row of module pads to contact the QSFP-DD connector.

The additional QSFP-DD pads have an 'A' label in Table 1 to designate them as the first row of module pads to contact the QSFP-DD connector. The additional QSFP-DD pads have first, second and third mate to the connector pins for both insertion and removal. Each of the first, second and third mate connections of the legacy QSFP+/QSFP28 pads and the respective additional QSFP-DD pads are simultaneous.

Figure 2 shows the signal symbols and pad numbering for the QSFP-DD module edge connector. The diagram shows the module PCB edge as a top and bottom view. There are 76 pads intended for high speed signals, low speed signals, power and ground connections.

Table 1 provides more information about each of the 76 pads. Figure 36 and Figure 37 show pad dimensions. The connector can be integrated into a 2x1 stacked configuration with 2 ports as illustrated in Figure 24 or a surface mount configuration as shown in Figure 25.

For EMI protection the signals from the host connector should be shut off when the QSFP-DD module is not present. Standard board layout practices such as connections to Vcc and GND with vias, use of short and equal-length differential signal lines are recommended. The chassis ground (case common) of the QSFP-DD module should be isolated from the module's circuit ground, GND, to provide the equipment designer flexibility regarding connections between external electromagnetic interference shields and circuit ground, GND, of the module.

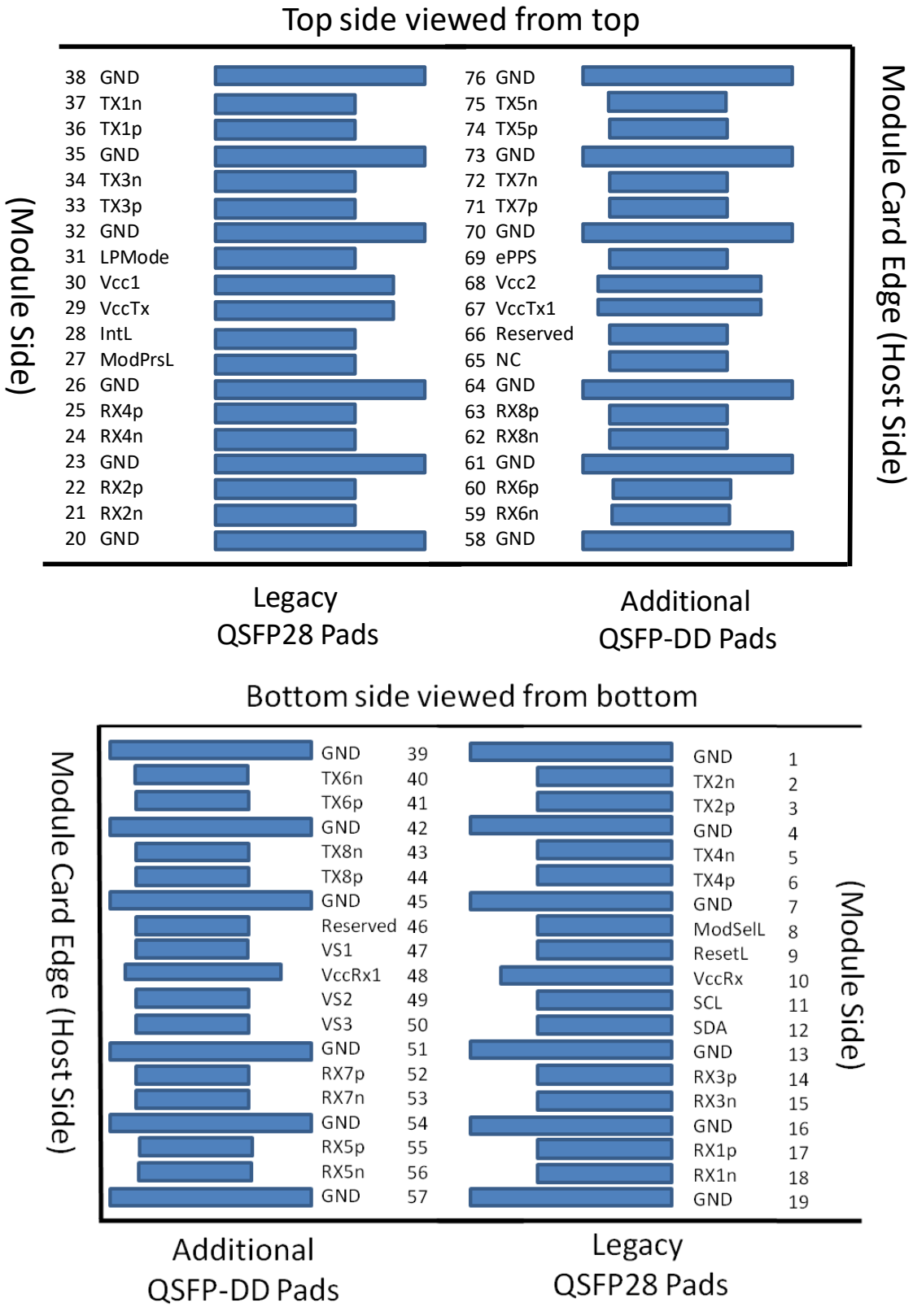


Figure 2: Module pad layout

Table 1- Pad Function Definition

Pad	Logic	Symbol	Description	Plug Sequence[4]	Notes
1		GND	Ground	1B	1
2	CML-I	Tx2n	Transmitter Inverted Data Input	3B	
3	CML-I	Tx2p	Transmitter Non-Inverted Data Input	3B	
4		GND	Ground	1B	1
5	CML-I	Tx4n	Transmitter Inverted Data Input	3B	
6	CML-I	Tx4p	Transmitter Non-Inverted Data Input	3B	
7		GND	Ground	1B	1
8	LVTTL-I	ModSelL	Module Select	3B	
9	LVTTL-I	ResetL	Module Reset	3B	
10		VccRx	+3.3V Power Supply Receiver	2B	2
11	LVCMOS-I/O	SCL	2-wire serial interface clock	3B	
12	LVCMOS-I/O	SDA	2-wire serial interface data	3B	
13		GND	Ground	1B	1
14	CML-O	Rx3p	Receiver Non-Inverted Data Output	3B	
15	CML-O	Rx3n	Receiver Inverted Data Output	3B	
16		GND	Ground	1B	1
17	CML-O	Rx1p	Receiver Non-Inverted Data Output	3B	
18	CML-O	Rx1n	Receiver Inverted Data Output	3B	
19		GND	Ground	1B	1
20		GND	Ground	1B	1
21	CML-O	Rx2n	Receiver Inverted Data Output	3B	
22	CML-O	Rx2p	Receiver Non-Inverted Data Output	3B	
23		GND	Ground	1B	1
24	CML-O	Rx4n	Receiver Inverted Data Output	3B	
25	CML-O	Rx4p	Receiver Non-Inverted Data Output	3B	
26		GND	Ground	1B	1
27	LVTTL-O	ModPrsL	Module Present	3B	
28	LVTTL-O	IntL	Interrupt	3B	
29		VccTx	+3.3V Power supply transmitter	2B	2
30		Vcc1	+3.3V Power supply	2B	2
31	LVTTL-I	LPMode	Low Power mode	3B	
32		GND	Ground	1B	1
33	CML-I	Tx3p	Transmitter Non-Inverted Data Input	3B	
34	CML-I	Tx3n	Transmitter Inverted Data Input	3B	
35		GND	Ground	1B	1
36	CML-I	Tx1p	Transmitter Non-Inverted Data Input	3B	
37	CML-I	Tx1n	Transmitter Inverted Data Input	3B	
38		GND	Ground	1B	1

Pad	Logic	Symbol	Description	Plug Sequence[4]	Notes
39		GND	Ground	1A	1
40	CML-I	Tx6n	Transmitter Inverted Data Input	3A	
41	CML-I	Tx6p	Transmitter Non-Inverted Data Input	3A	
42		GND	Ground	1A	1
43	CML-I	Tx8n	Transmitter Inverted Data Input	3A	
44	CML-I	Tx8p	Transmitter Non-Inverted Data Input	3A	
45		GND	Ground	1A	1
46		Reserved	For future use	3A	3
47		VS1	Module Vendor Specific 1	3A	3
48		VccRx1	3.3V Power Supply	2A	2
49		VS2	Module Vendor Specific 2	3A	3
50		VS3	Module Vendor Specific 3	3A	3
51		GND	Ground	1A	1
52	CML-O	Rx7p	Receiver Non-Inverted Data Output	3A	
53	CML-O	Rx7n	Receiver Inverted Data Output	3A	
54		GND	Ground	1A	1
55	CML-O	Rx5p	Receiver Non-Inverted Data Output	3A	
56	CML-O	Rx5n	Receiver Inverted Data Output	3A	
57		GND	Ground	1A	1
58		GND	Ground	1A	1
59	CML-O	Rx6n	Receiver Inverted Data Output	3A	
60	CML-O	Rx6p	Receiver Non-Inverted Data Output	3A	
61		GND	Ground	1A	1
62	CML-O	Rx8n	Receiver Inverted Data Output	3A	
63	CML-O	Rx8p	Receiver Non-Inverted Data Output	3A	
64		GND	Ground	1A	1
65		NC	No Connect	3A	3
66		Reserved	For future use	3A	3
67		VccTx1	3.3V Power Supply	2A	2
68		Vcc2	3.3V Power Supply	2A	2
69	LVTTL-I	ePPS	Precision Time Protocol (PTP) reference clock input	3A	3
70		GND	Ground	1A	1
71	CML-I	Tx7p	Transmitter Non-Inverted Data Input	3A	
72	CML-I	Tx7n	Transmitter Inverted Data Input	3A	
73		GND	Ground	1A	1
74	CML-I	Tx5p	Transmitter Non-Inverted Data Input	3A	
75	CML-I	Tx5n	Transmitter Inverted Data Input	3A	
76		GND	Ground	1A	1

Note 1: QSFP-DD uses common ground (GND)for all signals and supply (power). All are common within the QSFP-DD module and all module voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal-common ground plane.

Note 2: VccRx, VccRx1, Vcc1, Vcc2, VccTx and VccTx1 shall be applied concurrently. Requirements defined for the host side of the Host Card Edge Connector are listed in Table 8. VccRx, VccRx1, Vcc1, Vcc2, VccTx and VccTx1 may be internally connected within the module in any combination. For power classes 4 and above the module differential loading of input voltage pins must not result in exceeding pin current limits. The connector Vcc pins are each rated for a maximum current of 1000 mA.

Note 3: All Vendor Specific, Reserved, No Connect and ePPS (if not used) pins may be terminated with 50 Ω to ground on the host. Pad 65 (No Connect) shall be left unconnected within the module. Vendor specific and Reserved pads shall have an impedance to GND that is greater than 10 kΩ and less than 100 pF.

Note 4: Plug Sequence specifies the mating sequence of the host connector and module. The sequence is 1A, 2A, 3A, 1B, 2B, 3B. (see Figure 2 for pad locations) Contact sequence A will make, then break contact with additional QSFP-DD pads. Sequence 1A and 1B will then occur simultaneously, followed by 2A and 2B, followed by 3A and 3B.

4.2 Low Speed Electrical Hardware Signals

In addition to the 2-wire serial interface the module has the following low speed signals for control and status:

- ModSelL
- ResetL
- LPMode
- ModPrsL
- IntL
- ePPS.

4.2.1 ModSelL

The ModSelL is an input signal that shall be pulled to Vcc in the QSFP-DD module (see Table 2). When held low by the host, the module responds to 2-wire serial communication commands. The ModSelL allows the use of multiple QSFP-DD modules on a single 2-wire interface bus. When ModSelL is “High”, the module shall not respond to or acknowledge any 2-wire interface communication from the host.

In order to avoid conflicts, the host system shall not attempt 2-wire interface communications within the ModSelL de-assert time after any QSFP-DD modules are deselected. Similarly, the host must wait at least for the period of the ModSelL assert time before communicating with the newly selected module. The assertion and de-asserting periods of different modules may overlap as long as the above timing requirements are met.

4.2.2 ResetL

The ResetL signal shall be pulled to Vcc in the module (see Table 2). A low level on the ResetL signal for longer than the minimum pulse length (t_Reset_init) (See Table 4) initiates a complete module reset, returning all user module settings to their default state.

4.2.3 LPMode

LPMode is an input signal. The LPMode signal shall be pulled up to Vcc in the QSFP-DD module (see Table 2). LPMode is used in the control of the module power mode, see CMIS 4.0 Chapter 6.3.1.3.

4.2.4 ModPrsL

ModPrsL shall be pulled up to Vcc Host on the host board and pulled low in the module (see Table 2). The ModPrsL is asserted “Low” when the module is inserted. The ModPrsL is deasserted “High” when the module is physically absent from the host connector due to the pull-up resistor on the host board.

4.2.5 IntL

IntL is an output signal. The IntL signal is an open collector output and shall be pulled to Vcc Host on the host board (see Table 2). When the IntL signal is asserted Low it indicates a change in module state, a possible module operational fault or a status critical to the host system. The host identifies the source of the interrupt using the 2-wire serial interface. The IntL signal is deasserted “High” after all set interrupt flags are read.

4.2.6 ePPS PTP Reference Clock (Optional)

For high-performance Precision Time Protocol (PTP) applications, a PTP reference clock with Pulse Per Second modulation, (Enhanced Pulse Per Second (ePPS)) may be provided from the host to the module. This can be used for either offline delay characterization or real-time delay compensation within the module. The clock is used to synchronize tightly the Host Time-of-Day counter to the module internal Time-of-Day Counter.

Editor’s Note – Full definition of ePPS is currently under development.

4.3 Examples of QSFP-DD Host Board Schematic

Figure 3, Figure 4 and Figure 5 show examples of QSFP-DD host PCB schematics with connections to CDR and control ICs. An 8-wide electrical/optical interface is shown. Note alternate electrical/optical interfaces are supported using optical multiplexing (WDM) or electrical multiplexing.

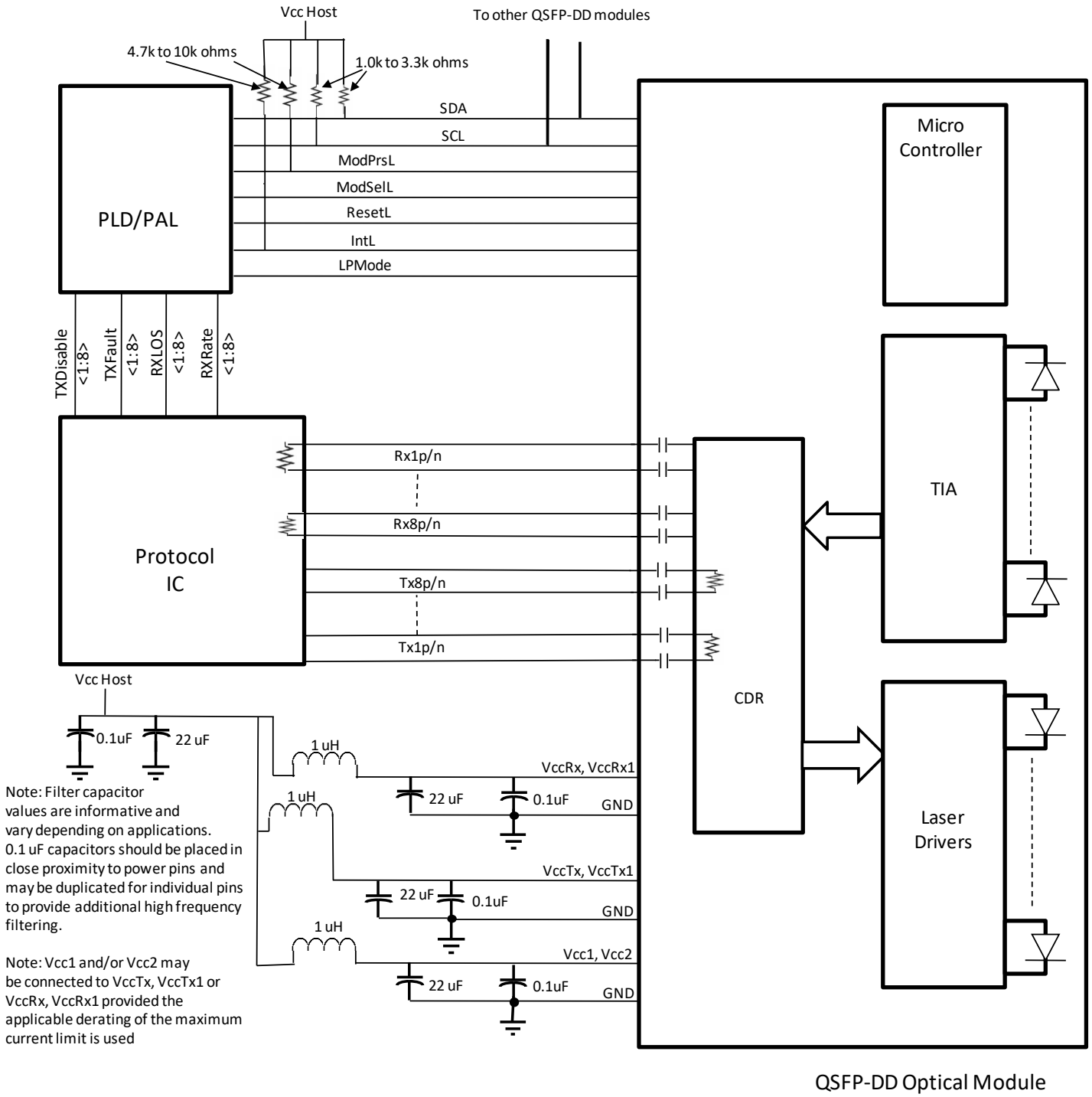


Figure 3: Example QSFP-DD Host Board Schematic for Optical Modules

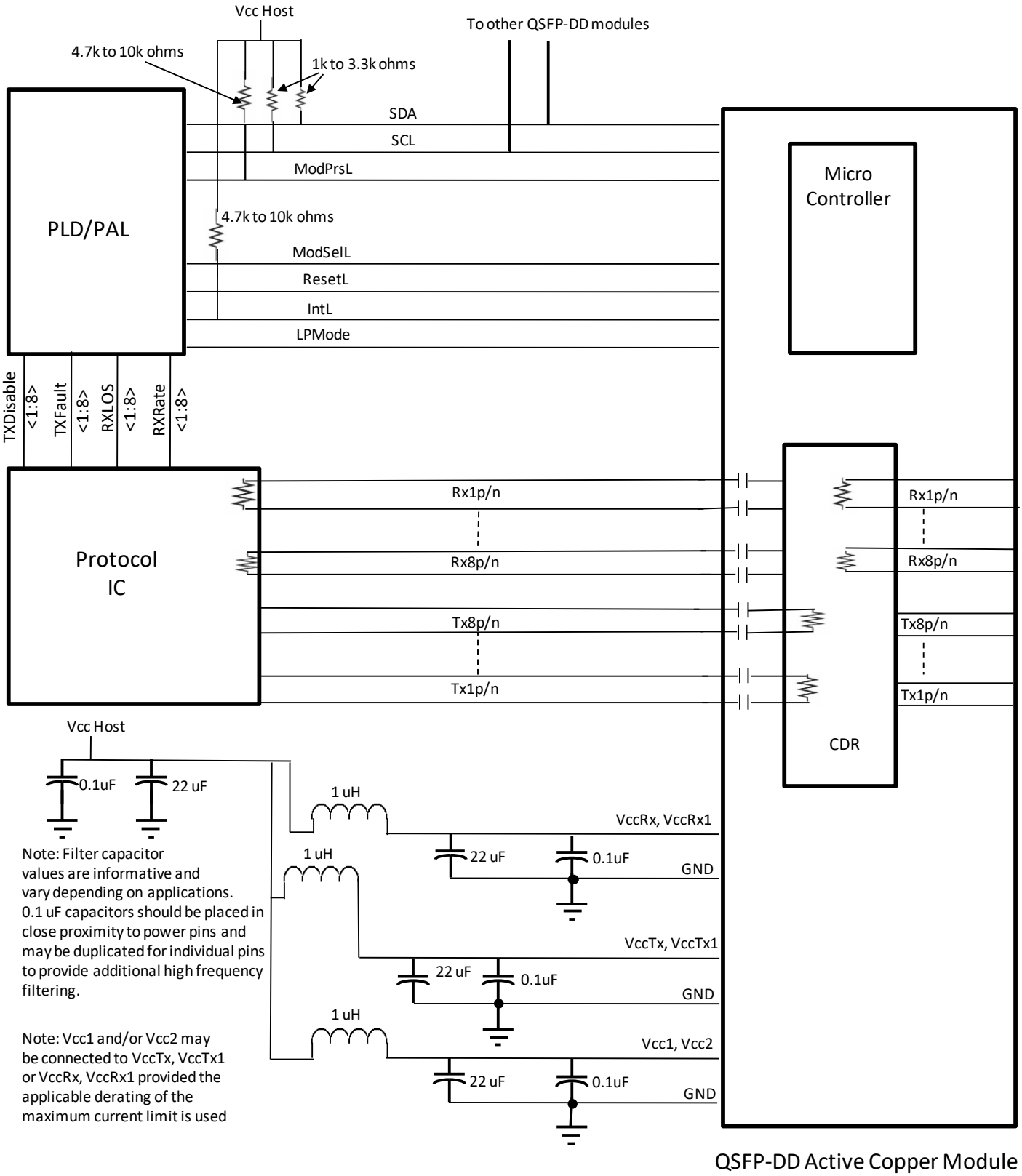


Figure 4: Example QSFP-DD Host Board Schematic for active copper cables

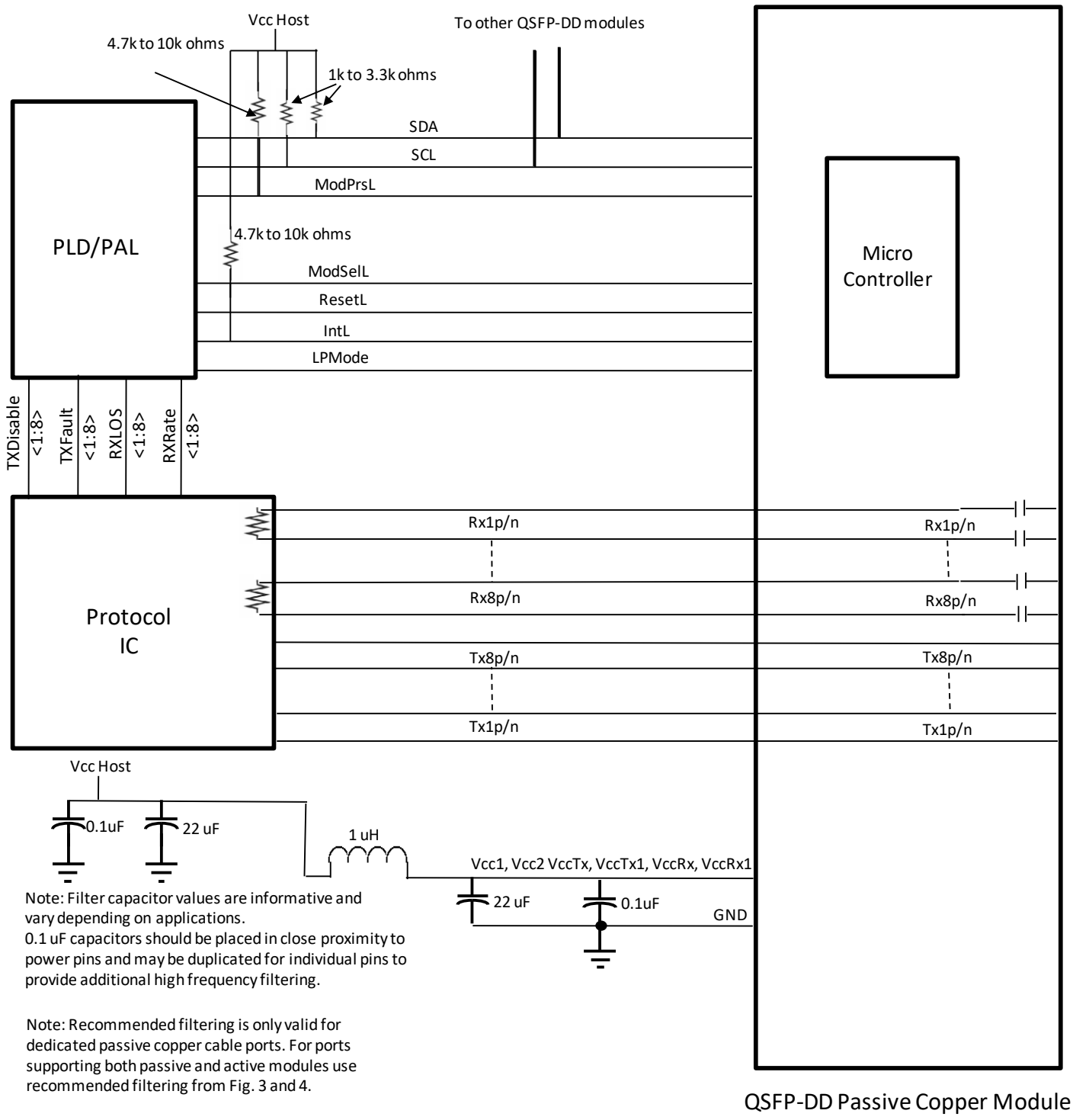


Figure 5: Example QSFP-DD Host Board Schematic for passive copper cables

4.4 Low Speed Electrical Specification

4.4.1 TWI Logic Levels and Bus Loading

Low speed signaling other than the SCL and SDA interface is based on Low Voltage TTL (LVTTL) operating at Vcc. Vcc refers to the generic supply voltages of VccTx, VccRx, Vcc host or Vcc1. Hosts shall use a pull-up resistor connected to Vcc host on each of the 2-wire interface SCL (clock), SDA (data), and all low speed status outputs (see Table 2). The SCL and SDA is a hot plug interface that may support a bus topology. During module insertion or removal, the module may implement a pre-charge circuit which prevents corrupting data transfers from other modules that are already using the bus.

Tradeoffs between pull-up resistor values total bus capacitance and the estimated bus rise/fall times are shown Figure 6.

The QSFP-DD low speed electrical specifications are given in Table 2. Implementations compliant to this specification ensures compatibility between host bus masters and the 2-wire interface.

Table 2- Low Speed Control and Sense Signals

Parameter	Symbol	Min	Max	Unit	Condition
SCL and SDA	VOL	0	0.4	V	IOL (max)=3 mA for fast mode, 20 mA for Fast-mode plus
SCL and SDA	VIL	-0.3	Vcc*0.3	V	
	VIH	VCC*0.7	Vcc+0.5	V	
Capacitance for SCL and SDA I/O signal	Ci		14	pF	
Total bus capacitive load for SCL and SDA	Cb		100	pF	For 400 kHz clock rate use 3 kΩ pullup resistor, max. For 1000 kHz clock rate refer to Figure 6.
			200	pF	For 400 kHz clock rate use 1.6 kΩ pullup resistor, max. For 1000 kHz clock rate refer to Figure 6.
LPMode, ResetL, ModSelL and ePPS	VIL	-0.3	0.8	V	
	VIH	2	VCC+0.3	V	
LPMode, ResetL and ModSelL	|Iin|		360	μA	0V<Vin<Vcc
ePPS	|Iin|		TBD	μA	0V<Vin<Vcc
IntL	VOL	0	0.4	V	IOL=2.0 mA
	VOH	VCC-0.5	VCC+0.3	V	10 kΩ pull-up to Host Vcc
ModPrsL	VOL	0	0.4	V	IOL=2.0 mA
	VOH				ModPrsL can be implemented as a short-circuit to GND on the module

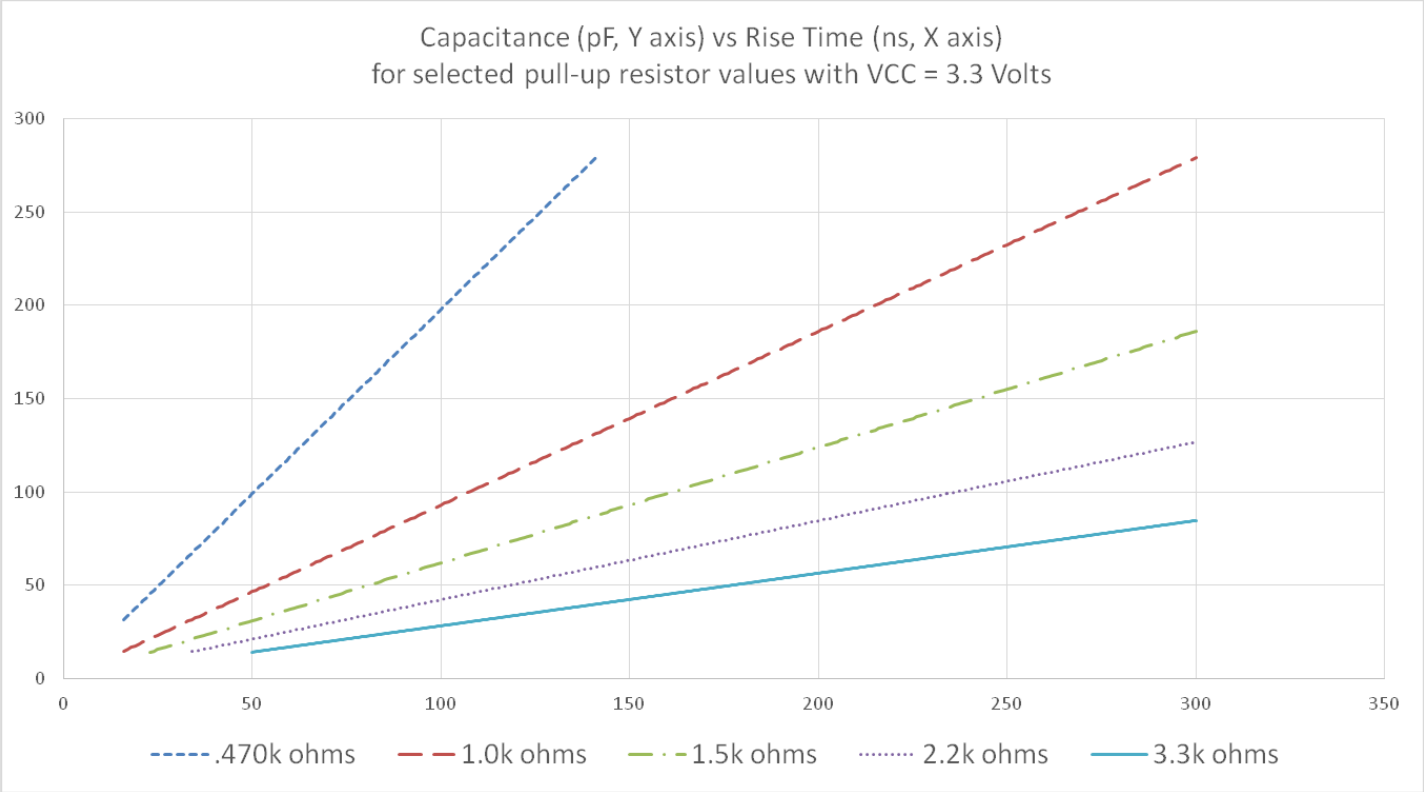


Figure 6: SDA/SCL options for pull-up resistor, bus capacitance and rise/fall times

4.5 Management Interface

A management interface, as already commonly used in other form factors like QSFP, SFP, and CDFP, is specified in order to enable flexible use of the module by the user. The memory map for QSFP-DD is found in the "Common Management Interface Specification (CMIS)" (see www.QSFP-DD.com). Some timing requirements are critical, especially for a multi-channel device, so the interface speed may optionally be increased. Byte 00h on the Lower Page or Address 128 Page 00h is used to indicate the use of the QSFP-DD memory map rather than the QSFP memory map. When a QSFPxx module is inserted into a QSFP-DD port the host must determine which memory map to use (e.g. SFF-8636 or CMIS) based on the QSFP identifier at Byte 00h on the Lower Page or Address 128 Page 00h. This case is outside the scope of this document.

In some applications, muxing or demuxing may occur in the module. In this specification, all references to channel numbers are based on the electrical connector interface channels, unless otherwise indicated. In cases where a status or control aspect is applicable only to channels after muxing or demuxing has occurred, the status or control is intended to apply to all channels in the mux group, unless otherwise indicated.

Low speed signaling is based on Low Voltage CMOS (LVCMOS) operating at Vcc. Hosts shall use a pull-up resistor connected to Vcc_host on the 2-wire interface SCL (clock) and SDA (Data) signals. Detailed electrical specifications are given in 4.4. Timing specifications for management functionality involving electrical low speed signals are found are given in Table 4.

Nomenclature for all registers more than 1 bit long is MSB-LSB.

4.5.1 Management Interface Timing Specification

The timing parameters for the 2-Wire interface to the QSFP-DD module and the QSFP-DD memory transaction timings are shown in Figure 7 and specified in Table 3. The default clock rate is a maximum of 400 kHz with an option to support up to a maximum of 1 MHz. This clause closely follows the QSFP+ SFF-8636 specification.

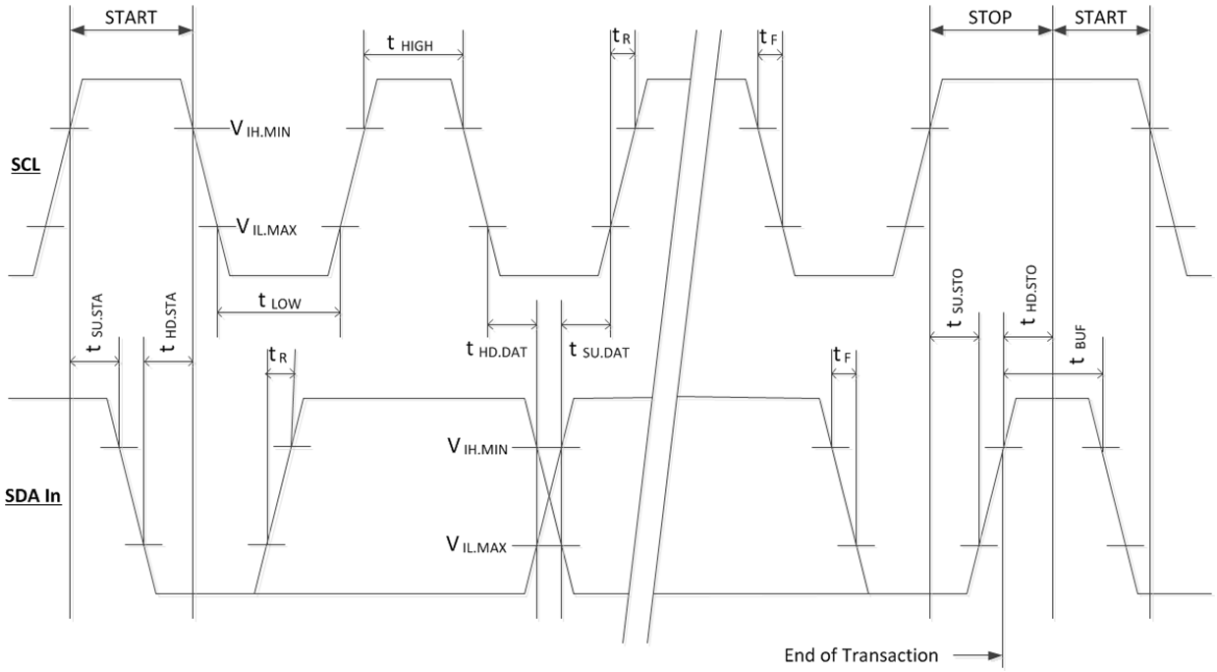


Figure 7: QSFP-DD TWI Timing Diagram

Table 3- Management Interface timing parameters

TWI Modes		Fast Mode (400 kHz)		Fast Mode Plus (1 MHz)			
Parameter	Symbol	Min	Max	Min	Max	Unit	Conditions
Clock Frequency	fSCL	0	400	0	1000	kHz	
Clock Pulse Width Low	tLOW	1.3		0.50		µs	
Clock Pulse Width High	tHIGH	0.6		0.26		µs	
Time bus free before new transmission can start	tBUF	20		20		µs	Between STOP and START and between ACK and ReStart
START Hold Time	tHD.STA	0.6		0.26		µs	The delay required between SDA becoming low and SCL starting to go low in a START
START Setup Time	tSU.STA	0.6		0.26		µs	The delay required between SCL becoming high and SDA starting to go low in a START
Data In Hold Time	tHD.DAT	0		0		µs	
Data In Setup Time	tSU.DAT	0.1		0.1		µs	
Input Rise Time	tR		300		120	ns	From (VL,MAX=0.3*Vcc) to (VIH,MIN=0.7*Vcc), see Figure 6
Input Fall Time	tF		300		120	ns	From (VIH,MIN=0.7*Vcc) to (VIL,MAX=0.3*Vcc), see Figure 6
STOP Setup Time	tSU.STO	0.6		0.26		µs	
STOP Hold Time	tHD.STO	0.6		0.26		µs	
Aborted sequence – bus release	Deselect _Abort		2		2	ms	Delay from a host de-asserting ModSelL (at any point in a bus sequence) to the QSFP-DD module releasing SCL and SDA
ModSelL Setup Time[1]	tSU. ModSelL	2		2		ms	ModSelL Setup Time is the setup time on the select line before the start of a host initiated serial bus sequence.
ModSelL Hold Time[1]	tHD. ModSelL	2		2		ms	ModSelL Hold Time is the delay from completion of a serial bus sequence to changes of module select status.
Serial Interface Clock Holdoff “Clock Stretching”	T_clock_hold		500		500	µs	Time the QSFP-DD module may hold the SCL line low before continuing with a read or write operation.
Complete Single or Sequential Write to non-volatile registers	tWR		80		80	ms	Time to complete a Single or Sequential Write to non-volatile registers.
Accept a single or sequential write to volatile memory	tNACK		10		10	ms	Time to complete a Single or Sequential Write to volatile registers.
Time to complete a memory bank/page	tBPC		10		10	ms	Time to complete a memory bank and/or page change.
Endurance (Write Cycles)		50K		50k		cycles	Module Case Temperature = 70 ºC
Note 1: When the host has determined that module is QSFP-DD, the management registers can be read to determine alternate supported ModSelL set up and hold times.							

The 2-wire serial interface address of the QSFP-DD module is 1010000X (A0h). In order to allow access to multiple QSFP-DD modules on the same 2-wire serial bus, the QSFP-DD includes a module select pad, ModSelL. This input (which is pulled high, deselected in the module) must be held low by the host to select the module of interest and allow communication over the 2-wire serial interface. The module must not respond to or accept 2-wire serial bus instructions unless it is selected.

Before initiating a 2-wire serial bus communication, the host shall provide setup time on the ModSelL line of all modules on the 2-wire bus. The host shall not change the ModSelL line of any module until the 2-wire serial bus communication is complete and the hold time requirement is satisfied.

4.5.1.1 Bus timing tBUF

The timing attribute tBUF is the bus free time between sequential TWI transactions, see Figure 7. It's measured from the low to high SDA edge of the Stop condition of the Write transaction to the high to low SDA edge of the Start condition for the next transaction.

4.5.1.2 Bus timing tWR

The timing attribute tWR is the time required for a module to complete its internally timed write cycle after a single or sequential write to non-volatile memory before the next basic management operation can be accepted, see Figure 8. It's measured from the low to high SDA edge of the Stop condition of the Write transaction to the high to low SDA edge of the Start condition for the next transaction.

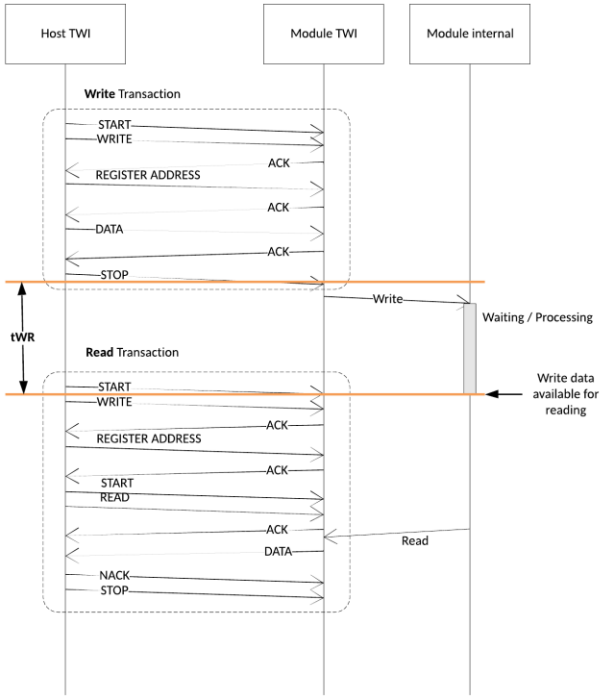


Figure 8: Bus timing tWR

4.5.1.3 Bus timing tNACK

The timing attribute tNACK is the time required for a module to complete its internally timed write cycle after a single or sequential write to volatile memory before the next basic management operation can be accepted, see Figure 9. It's measured from the low to high SDA edge of the Stop condition of the Write transaction to the high to low SDA edge of the Start condition for the next transaction.

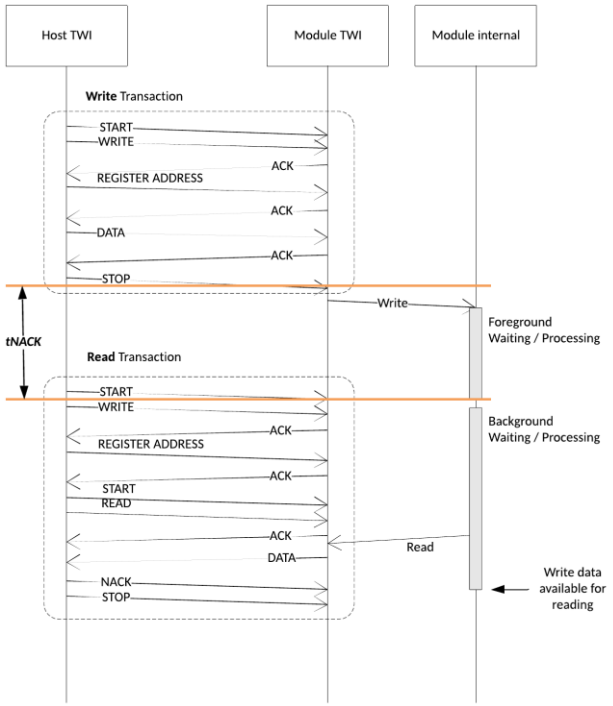


Figure 9: Bus timing tNACK

4.5.1.4 Bus timing tBPC

The timing attribute tBPC is the time required for a module to complete the change for the requested Bank and/or Page selection, see Figure 10. It's measured from the low to high SDA edge of the Stop condition of the Write transaction to the high to low SDA edge of the Start condition for the next transaction.

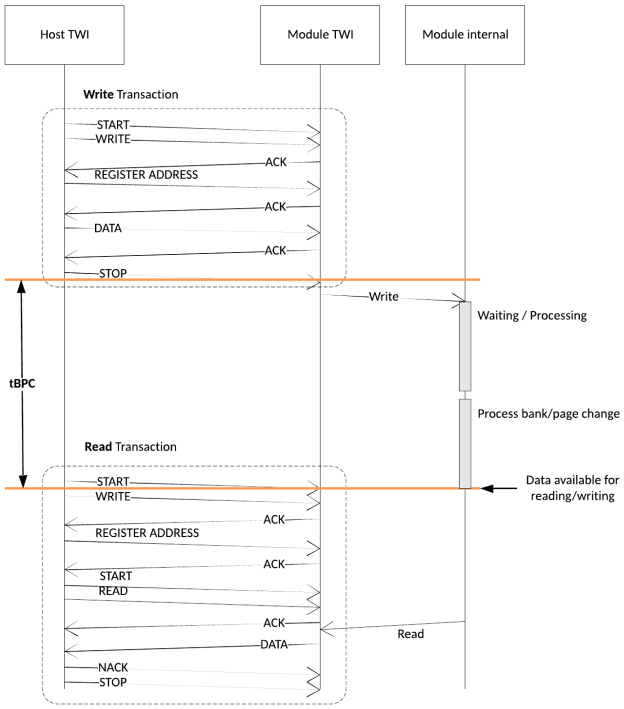


Figure 10: Bus timing tBPC

4.5.2 Timing for soft control and status functions

Timing for QSFP-DD soft control status functions are described in Table 4. Squelch and disable timings are defined in Table 5.

Table 4- Timing for QSFP-DD soft control and status functions

Parameter	Symbol	Min	Max	Unit	Conditions
MgmtInitDuration	Max MgmtInit Duration		2000	ms	Time from power on[1], hot plug or rising edge of reset until until the high to low SDA transition of the Start condition for the first acknowledged TWI transaction.
ResetL Assert Time	t_reset_init	10		µs	Minimum pulse time on the ResetL signal to initiate a module reset.
IntL Assert Time	ton_IntL		200	ms	Time from occurrence of condition triggering IntL until Vout:IntL=Vol
IntL Deassert Time	toff_IntL		500	µs	Time from clear on read[2] operation of associated flag until Vout:IntL=Voh. This includes deassert times for Rx LOS, Tx Fault and other flag bits.
Rx LOS Assert Time	ton_los		100	ms	Time from Rx LOS condition present to Rx LOS bit set (value = 1b) and IntL asserted.
Rx LOS Assert Time (optional fast mode)	ton_losf		1	ms	Time from Rx LOS state to Rx LOS bit set (value = 1b) and IntL asserted.
Tx Fault Assert Time	ton_Txfault		200	ms	Time from Tx Fault state to Tx Fault bit set (value=1b) and IntL asserted.
Flag Assert Time	ton_flag		200	ms	Time from occurrence of condition triggering flag to associated flag bit set (value=1b) and IntL asserted.
Mask Assert Time	ton_mask		100	ms	Time from mask bit set (value=1b)[3] until associated IntL assertion is inhibited
Mask Deassert Time	toff_mask		100	ms	Time from mask bit cleared (value=0b)[3] until associated IntL operation resumes
Data Path Tx Turn On Max Duration[5]	DataPathTxTurnOn_MaxDuration				see CMIS memory P01h: B168
Data Path Tx Turn Off Max Duration[5]	DataPathTxTurnOff_MaxDuration				see CMIS memory P01h: B168
Data Path Deinit Max Duration[5]	DataPathDeinit_MaxDuration				see CMIS memory P01h: B144
Data Path Init Max Duration[5]	DataPathInit_MaxDuration				see CMIS memory P01h: B144
Module Pwr Up Max Duration[6]	ModulePwrUp_MaxDuration				see CMIS memory P01h: B167
Module Pwr Dn Max Duration[6]	ModulePwrDn_MaxDuration				see CMIS memory P01h: B167

Notes: 1. Power on is defined as the instant when supply voltages reach and remain at or above the minimum level specified in Table 8.

2. Measured from low to high SDA edge of the Stop condition of the read transaction.

3. Measured from low to high SDA edge of the Stop condition of the write transaction.

4. Rx LOS condition is defined at the optical input by the relevant standard.

5. Measured from the low to high SDA edge of the Stop condition of the Write transaction until the IntL for the state change Vout:IntL=Vol, unless the module advertises a less than 1 ms duration in which case there is no defined measurement.

6. Measured from the low to high SDA edge of the Stop condition of the Write transaction until the IntL for the state change Vout:IntL=Vol.

Table 5- I/O Timing for Squelch & Disable

Parameter	Symbol	Max	Unit	Conditions
Rx Squelch Assert Time	ton_Rxsq	15	ms	Time from loss of Rx input signal until the squelched output condition is reached, see 4.6.1.
Tx Squelch Assert Time	ton_Txsq	400	ms	Time from loss of Tx input signal until the squelched output condition is reached, see 4.6.2.
Tx Squelch Deassert Time	toff_Txsq	1.5	s	Tx squelch deassert is system and implementation dependent, see also 4.6.2.
Tx Disable Assert Time	ton_txdis	100	ms	Time from the stop condition of the Tx Disable write sequence[1] until optical output falls below 10% of nominal.
Tx Disable Assert Time (optional fast mode)	ton_txdisf	3	ms	Time from Tx Disable bit set (value = 1b)[1] until optical output falls below 10% of nominal and see notes 2 and 3.
Tx Disable Deassert Time	toff_txdis	400	ms	Time from Tx Disable bit cleared (value = 0b)[1] until optical output rises above 90% of nominal and see note 2.
Tx Disable Deassert Time (optional fast mode)	toff_txdisf	10	ms	Time from Tx Disable bit cleared (value = 0b)[1] until optical output rises above 90% of nominal, see note 3.
Rx Output Disable Assert Time	ton_rxdis	100	ms	Time from Rx Output Disable bit set (value = 1b)[1] until Rx output falls below 10% of nominal
Rx Output Disable Deassert Time	toff_rxdis	100	ms	Time from Rx Output Disable bit cleared (value = 0b)[1] until Rx output rises above 90% of nominal.
Squelch Disable Assert Time	ton_sqdis	100	ms	This applies to Rx and Tx Squelch and is the time from bit set (value = 0b)[1] until squelch functionality is disabled.
Squelch Disable Deassert Time	toff_sqdis	100	ms	This applies to Rx and Tx Squelch and is the time from bit cleared (value = 0b)[1] until squelch functionality is enabled.

Notes:
1. Measured from LOW to HIGH SDA signal transition of the STOP condition of the write transaction.
2. CMIS 4.0 and beyond the listed values are superseded by the advertised DataPathTxTurnOff_MaxDuration and DataPathTxTurnOn_MaxDuration times in P01h.168.
3. Listed values place a limit on the DataPathTxTurnOff_MaxDuration and DataPathTxTurnOn_MaxDuration times (P01h.168) that can be advertised by such modules (for CMIS 4.0 and beyond).

4.6 High Speed Electrical Specification

For detailed electrical specifications see the appropriate specification, e.g. IEEE Std 802.3-2018 Annex 86A, Annex 120E or Annex 120C, FC-PI-6, FC-PI-7, OIF-CEI-28G-VSR, OIF-CEI-56G-VSR or the InfiniBand specification. Partial or complete squelch specifications may be provided in the appropriate specification. Where squelch is not fully defined by the appropriate specification, the recommendations of the following subsections 4.6.1 and 4.6.2 may be used.

4.6.1 Rx(n)(p/n)

Rx(n)(p/n) are QSFP-DD module receiver data outputs. Rx(n)(p/n) are AC-coupled 100 Ohm differential lines that should be terminated with 100 Ohm differentially at the Host ASIC(SerDes). The AC coupling is inside the QSFP-DD module and not required on the Host board. When properly terminated, the differential voltage swing shall be less than or equal to 900 mVpp or the relevant standard, whichever is less.

Output squelch for loss of optical input signal, hereafter Rx Squelch, is required and shall function as follows. In the event of the Rx input signal on any optical port becoming equal to or less than the level required to assert LOS, then the receiver output(s) associated with that Rx port shall be squelched. A single Rx optical

port can be associated with more than one Rx output as shown in Table 9. In the squelched state output impedance levels are maintained while the differential voltage amplitude shall be less than 50 mVpp.

In normal operation the default case has Rx Squelch active. Rx Squelch can be deactivated using Rx Squelch Disable through the 2-wire serial interface. Rx Squelch Disable is an optional function.

4.6.2 Tx(n)(p/n)

Tx(n)(p/n) are QSFP-DD module transmitter data inputs. They are AC-coupled 100 Ohm differential lines with 100 Ohm differential terminations inside the QSFP-DD optical module. The AC coupling is implemented inside the QSFP-DD optical module and not required on the Host board.

Output squelch for loss of electrical signal, hereafter Tx Squelch, is an optional function. Where implemented it shall function as follows. In the event of the differential, peak-to-peak electrical signal amplitude on any electrical input channel becoming less than 70 mVpp, then the transmitter optical output associated with that electrical input channel shall be squelched and the associated TxLOS flag set. If multiple electrical input channels are associated with the same optical output channel, the loss of any of the incoming electrical input channels causes the optical output channel to be squelched.

For applications, e.g. Ethernet, where the transmitter off condition is defined in terms of average power, squelching by disabling the transmitter is recommended and for applications, e.g. InfiniBand, where the transmitter off condition is defined in terms of OMA, squelching the transmitter by setting the OMA to a low level is recommended.

In module operation, where Tx Squelch is implemented, the default case has Tx Squelch active. Tx Squelch can be deactivated using Tx Squelch Disable through the 2-wire serial interface. Tx Squelch and Tx Squelch Disable are optional functions.

4.7 Power Requirements

The power supply has six designated pins, VccTx, VccTx1, Vcc1, Vcc2, VccRx, VccRx1 in the connector. Vcc1 and Vcc2 are used to supplement VccTx, VccTx1, VccRx or VccRx1 at the discretion of the module vendor. Power is applied concurrently to these pins.

A host board together with the QSFP-DD module(s) forms an integrated power system. The host supplies stable power to the module. The module limits electrical noise coupled back into the host system and limits inrush charge/current during hot plug insertion.

All power supply requirements in Table 8 shall be met at the maximum power supply current. No power sequencing of the power supply is required of the host system since the module sequences the contacts in the order of ground, supply and signals during insertion.

4.7.1 Power Classes and Maximum Power Consumption

There are two power modes; Low Power Mode and High Power Mode, and eight power classes, Class 1 - Class 8. Module power classes are defined in Table 6 and module power specifications are provided in Table 8.

Since a wide range of module power classes exist, to avoid exceeding the system power supply limits and cooling capacity when a module is inserted into a system designed to accommodate only low power consumption modules, it is recommended that the host implement the state machine defined in the QSFP-DD Management Interface Specification and identify the power class of the module before allowing the module to go into High Power Mode.

Table 6- Power Classes

Power Class	Max Power (W)
1	1.5
2	3.5
3	7.0
4	8.0
5	10
6	12
7	14
8	>14

In general, the higher power classification levels are associated with higher data rates and longer reaches. The system designer is responsible for ensuring that the maximum case temperature does not exceed the case temperature requirements.

4.7.2 Host Board Power Supply Filtering

The specification of the host power supply filtering network is beyond the scope of this specification, particularly because of the wide range of module Power Classes. During power transient events, the host should ensure that that any neighboring modules sharing the same supply stay within their specified supply voltage limits. An example of host board power supply filtering is shown in Figure 11.

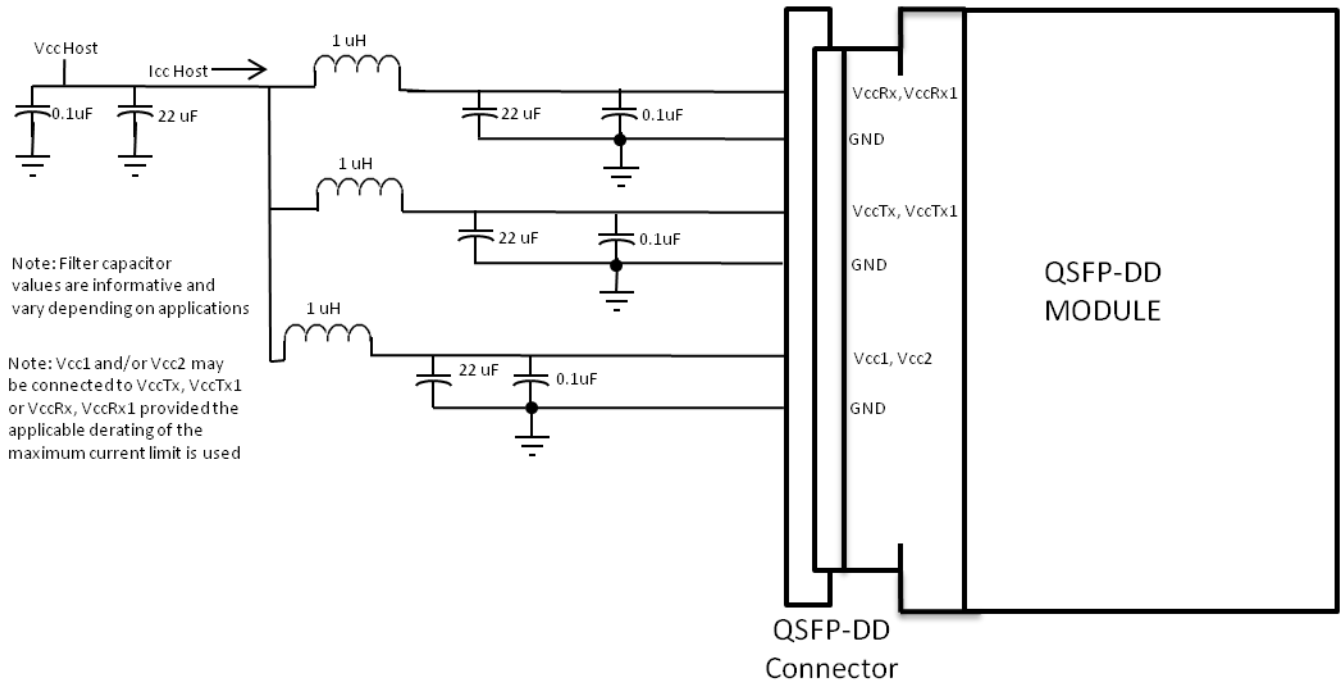


Figure 11: Recommended Host Board Power Supply Filtering

Any voltage drop across a filter network on the host is counted against the host DC set point accuracy specification. Inductors with DC Resistance of less than 0.1 Ohm should be used in order to maintain the required voltage at the Host Card Edge Connector. It is recommended that the 22 μF capacitors each have an equivalent series resistance of 0.22 Ohm.

The specifications for the power supply are shown in Table 8. The limits in Table 8 apply to the combined current that flows through all inductors in the power supply filter (represents host Icc current in Figure 11). The test method for measuring inrush current can be found in SFF-8679. Keysight Technologies application brief 5991-2778EN provides useful guidance.

4.7.3 Module Power Supply Specification

In order to avoid exceeding the host system power capacity, upon hot-plug, power cycle or reset, all QSFP-DD modules shall power up in Low Power Mode if LPMode is asserted. If LPMode is not asserted the module will proceed to High Power Mode without host intervention. Figure 12 shows waveforms for maximum instantaneous, sustained and steady state currents for Low Power and High Power modes. Specification values for maximum instantaneous, sustained and steady state currents at each power class are given in Table 8.

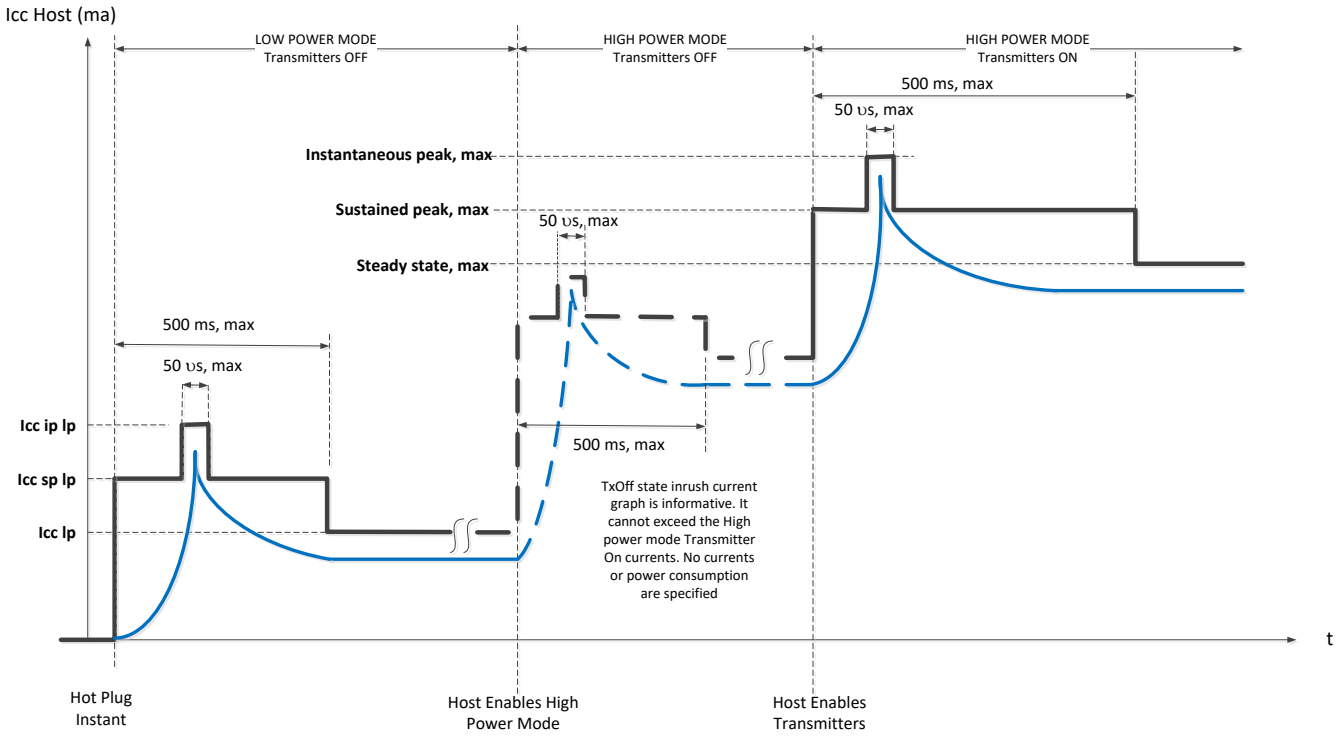


Figure 12: Instantaneous and sustained peak currents for Icc Host (see Table 8)

4.7.4 Host Board Power Supply Noise Output

The host shall generate an effective weighted integrated spectrum RMS noise less than the eN_Host value in Table 8 when tested by the methods of SFF-8431, D.17.1 with the following exception: The truncated function equation with coefficients from Table 7. The frequency response of the truncated function is illustrated in Figure 13.

Table 7- Truncated Filter Response Coefficients for Host Power Supply Noise Output

Frequency	a	b	c	d	e
10 Hz ≤ f ≤ 240.2 Hz	0	0	0	0	-0.1
240.2 Hz ≤ f ≤ 24.03 kHz	0.3784	-3.6045	12.694	-19.556	11.002
24.03 kHz ≤ f ≤ 360.4 kHz	-22.67038	430.392	-3053.779	9574.26	-11175.98
360.4 kHz ≤ f ≤ 12.6 MHz	3.692166	-91.467	838.80	-3400.38	5139.285
12.6 MHz ≤ f ≤ 24 MHz	0	0	0	0	-60

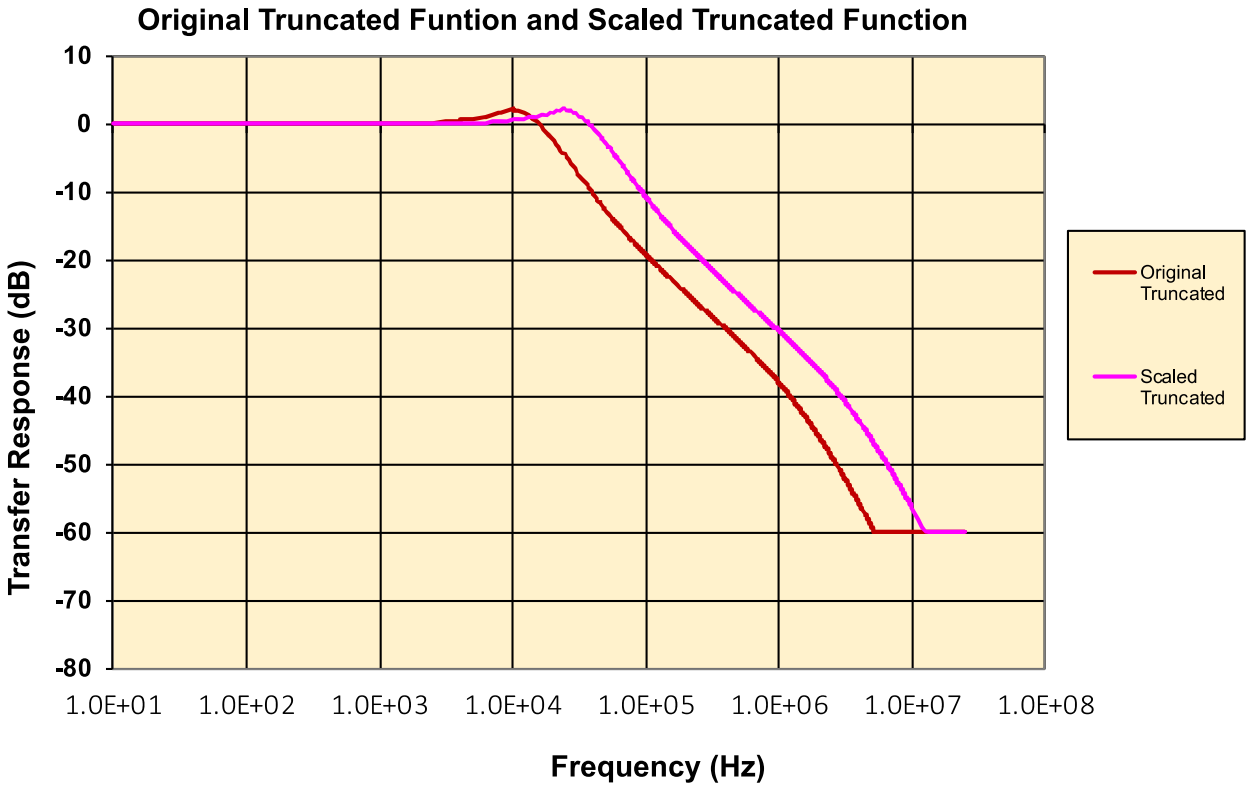


Figure 13: Truncated Transfer Response for Host Board Power Supply Noise Output measurement

4.7.5 Module Power Supply Noise Output

The QSFP-DD module shall generate less than the value in Table 8 when tested by the methods of SFF-8431, D.17.2. Note: The series resistor specified in D.17 Figure 56 is reduced for high power modules by the following equation: Rseries = 0.1*1.5/(Module Advertised Power Consumption (max)).

4.7.6 Module Power Supply Noise Tolerance

The QSFP-DD module shall meet all requirements and remain fully operational in the presence of a sinusoidal tolerance signal of amplitude given by Table 8, swept from 10 Hz to 10 MHz according to the methods of SFF-8431, D.17.3 with the exception that 4.7 μH in SFF-8431 Figure 58 is replaced with 1 uH and the ESR of the 22 μF capacitor (0.5 Ohm) is replaced with 0.22 Ohm. This emulates the worst case noise output of the host.

Table 8- Power Supply specifications, Instantaneous, sustained and steady state current limits

Parameter	Symbol	Min	Nom	Max	Unit
Power supply voltages VccTx, VccTx1, VccRx, VccRx1, Vcc1 & Vcc2 including ripple, droop and noise below 100 kHz[1]		3.135	3.3	3.465	V
Host RMS noise output 40 Hz-10 MHz (eN_Host)				25	mV
Module RMS noise output 10 Hz - 10 MHz				30	mV
Module power supply noise tolerance 10 Hz - 10 MHz (peak-to-peak)	$PSNR_{mod}$			66	mV
Module inrush - instantaneous peak duration[2]	T_ip			50	µs
Module inrush - initialization time[2]	T_init			500	ms
Low Power Mode					
Power Consumption	P_lp			1.5	W
Instantaneous peak current at hot plug	Icc_ip_lp	-	-	600	mA
Sustained peak current at hot plug	Icc_sp_lp	-	-	495	mA
Steady state current	Icc_lp	See Note 3			mA
High Power Mode Power Class 1 module					
Power Consumption	P_1			1.5	W
Instantaneous peak current	Icc_ip_1	-	-	600	mA
Sustained peak current	Icc_sp_1	-	-	495	mA
Steady state current	Icc_1	See Note 3			mA
High Power Mode Power Class 2 module					
Power Consumption	P_2			3.5	W
Instantaneous peak current	Icc_ip_2	-	-	1400	mA
Sustained peak current	Icc_sp_2	-	-	1155	mA
Steady state current	Icc_2	See Note 3			mA
High Power Mode Power Class 3 module					
Power Consumption	P_3			7	W
Instantaneous peak current	Icc_ip_3	-	-	2800	mA
Sustained peak current	Icc_sp_3	-	-	2310	mA
Steady state current	Icc_3	See Note 3			mA
High Power Mode Power Class 4 module					
Power Consumption	P_4			8	W
Instantaneous peak current	Icc_ip_4	-	-	3200	mA
Sustained peak current	Icc_sp_4	-	-	2640	mA
Steady state current	Icc_4	See Note 3			mA
High Power Mode Power Class 5 module					
Power Consumption	P_5			10	W
Instantaneous peak current	Icc_ip_5	-	-	4000	mA
Sustained peak current	Icc_sp_5	-	-	3300	mA
Steady state current	Icc_5	See Note 3			mA
High Power Mode Power Class 6 module					
Power Consumption	P_6			12	W
Instantaneous peak current	Icc_ip_6	-	-	4800	mA
Sustained peak current	Icc_sp_6	-	-	3960	mA
Steady state current	Icc_6	See Note 3			mA
High Power Mode Power Class 7 module					
Power Consumption	P_7			14	W
Instantaneous peak current	Icc_ip_7	-	-	5600	mA
Sustained peak current	Icc_sp_7	-	-	4620	mA
Steady state current	Icc_7	See Note 3			mA
High Power Mode Power Class 8 module					
Power Consumption	P_8[4]			>14	W
Instantaneous peak current	Icc_ip_8	-	-	P_8/2.5	A
Sustained peak current	Icc_sp_8	-	-	P_8/3.03	A
Steady state current	Icc_8	-	-	6	A

Notes: 1. Measured at VccTx, VccTx1, VccRx, VccRx1, Vcc1 and Vcc2.
2: T_ip and T_init are test conditions for measuring inrush current and not characteristics of the module
3: The module must stay within its declared power class.
4: User must read management register for maximum power consumption

4.8 ESD

Where ESD performance is not otherwise specified, e.g. in the InfiniBand specification, the QSFP-DD module shall meet ESD requirements given in EN61000-4-2, criterion B test specification when installed in a properly grounded cage and chassis. The units are subjected to 15kV air discharges during operation and 8kV direct contact discharges to the case. All the QSFP-DD module and host pins including high speed signal pins shall withstand 1000 V electrostatic discharge based on Human Body Model per ANSI/ESDA/JEDEC JS-001.

4.9 Clocking Considerations

4.9.1 Data Path Description

Within a module, host electrical and module media lanes are grouped together into a logical concept called a data path. A data path is intended to represent a group of lanes over which a block of data is distributed that will be powered up or down and initialized together. Some examples include a 100GAUI-4 to 100GBASE-SR4 module implementation, where the data path would include four host electrical lanes and four module media lanes, or a 400GAUI-8 to 400GBASE-DR4 module implementation, where the data path would include eight host electrical lanes and four module media lanes.

4.9.2 TX Clocking Considerations

Within a given Tx data path the host is responsible for ensuring that all electrical lanes delivered to the module are frequency synchronous (sourced from the same clock domain). If a module supports multiple Tx data paths running concurrently, the different Tx data paths can either all be in a single clock domain or separate clock domains. The module advertises which of these two modes it supports via the management registers.

If the module supports multiple Tx data paths running concurrently in a single clock domain, the module shall ensure that active Tx data paths continue to operate undisturbed even as other Tx data paths (and their associated Tx input lanes) are enabled/disabled by the host.

4.9.3 Rx Clocking Considerations

Within a given Rx data path all lanes received on the module media interface are required to be frequency synchronous (sourced from the same clock domain). If a module supports multiple Rx data paths running concurrently, the module shall allow the different Rx data paths to be asynchronous from each other (sourced from separate clock domains).

5 Optical Port Mapping and Optical Interfaces

5.1 Electrical data input/output to optical port mapping

Table 9 defines the mapping of electrical TX data inputs and Rx data outputs to optical ports. Note that there is no defined mapping of electrical input/output to optical wavelengths for WDM applications.

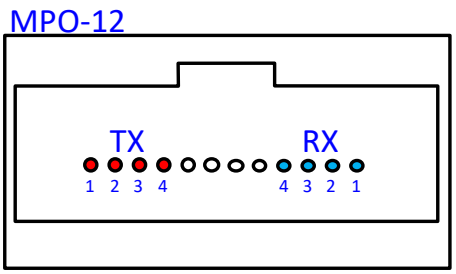
Table 9- Electrical Signal to Optical Port Mapping

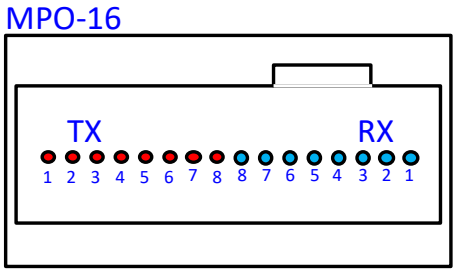
Electrical data input/output	Optical port mapping (see Figure 14)				
	LC, CS, SN, MDC	MPO-12, CS, SN, MDC	MPO-12, SN, MDC	MPO-12 (two row) MPO-16	MPO-12, SN, MDC, BiDi
	1 TX fiber 1 RX fiber [1]	2 TX fibers 2 RX fibers [1]	4 TX fibers 4 RX fibers [1]	8 TX fibers 8 RX fibers [1,3]	8 Tx (Rx) fibers [2,3]
Tx1	TX-1	TX-1	TX-1	TX-1	TR1
Tx2				TX-2	RT1
Tx3			TX-2	TX-3	TR2
Tx4				TX-4	RT2
Tx5		TX-2	TX-3	TX-5	TR3
Tx6				TX-6	RT3
Tx7			TX-4	TX-7	TR4
Tx8				TX-8	RT4
Rx1	RX-1	RX-1	RX-1	RX-1	RT1
Rx2				RX-2	TR1
Rx3			RX-2	RX-3	RT2
Rx4				RX-4	TR2
Rx5		RX-2	RX-3	RX-5	RT3
Rx6				RX-6	TR3
Rx7			RX-4	RX-7	RT4
Rx8				RX-8	TR4

Notes:
1. TX-n or RX-n where n is the optical port number as defined Figure 14.
2. TRn or RTn where n is the optical port number as defined Figure 14.
3. Some QSFP-DD modules may require fewer CS, SN, or MDC connectors. In such cases, Port #1 is always the left-most port. Successive ports then follow sequentially from left-to-right as shown in Figure 14.

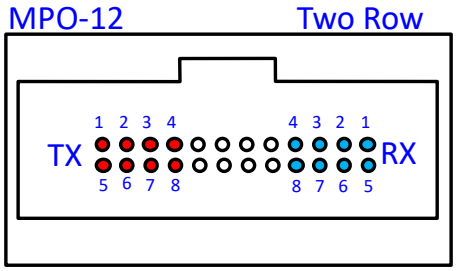
5.2 Optical Interfaces

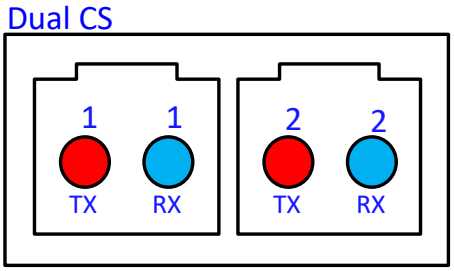
The recommended location and numbering of the optical ports for 12 Media Dependent Interfaces (MDI) are shown in Figure 14. The transmit and receive optical lanes shall occupy the positions depicted in Figure 14 when looking into the MDI receptacle with the connector keyway feature on top. QSFP-DD optical MDI examples are shown for three male MPO receptacles (see Figure 15, Figure 16, and Figure 17) a dual LC (see Figure 18), a CS connector (see Figure 19), a quad SN receptacle (see Figure 20), a quad MDC receptacle (see Figure 21), a dual SN receptacle (see Figure 22), and a dual MDC receptacle (see Figure 23).

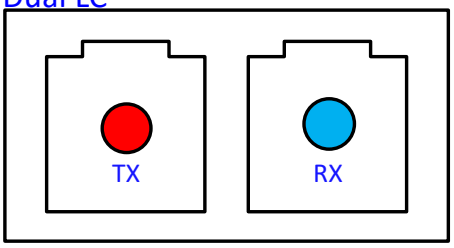


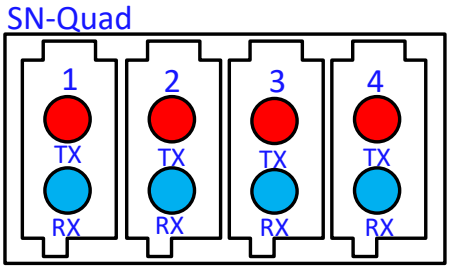


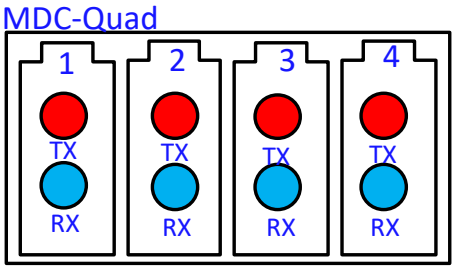
Note: The MPO 12, 2 row optical MDI is used for breakout applications and is not intended for structured cabling applications.

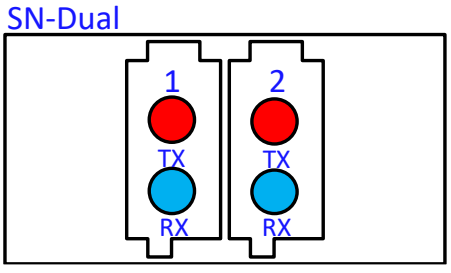


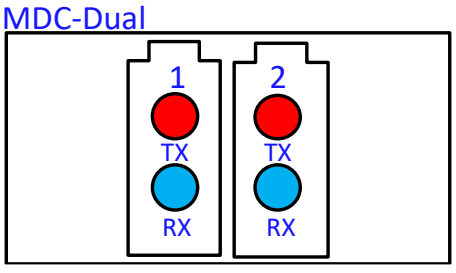


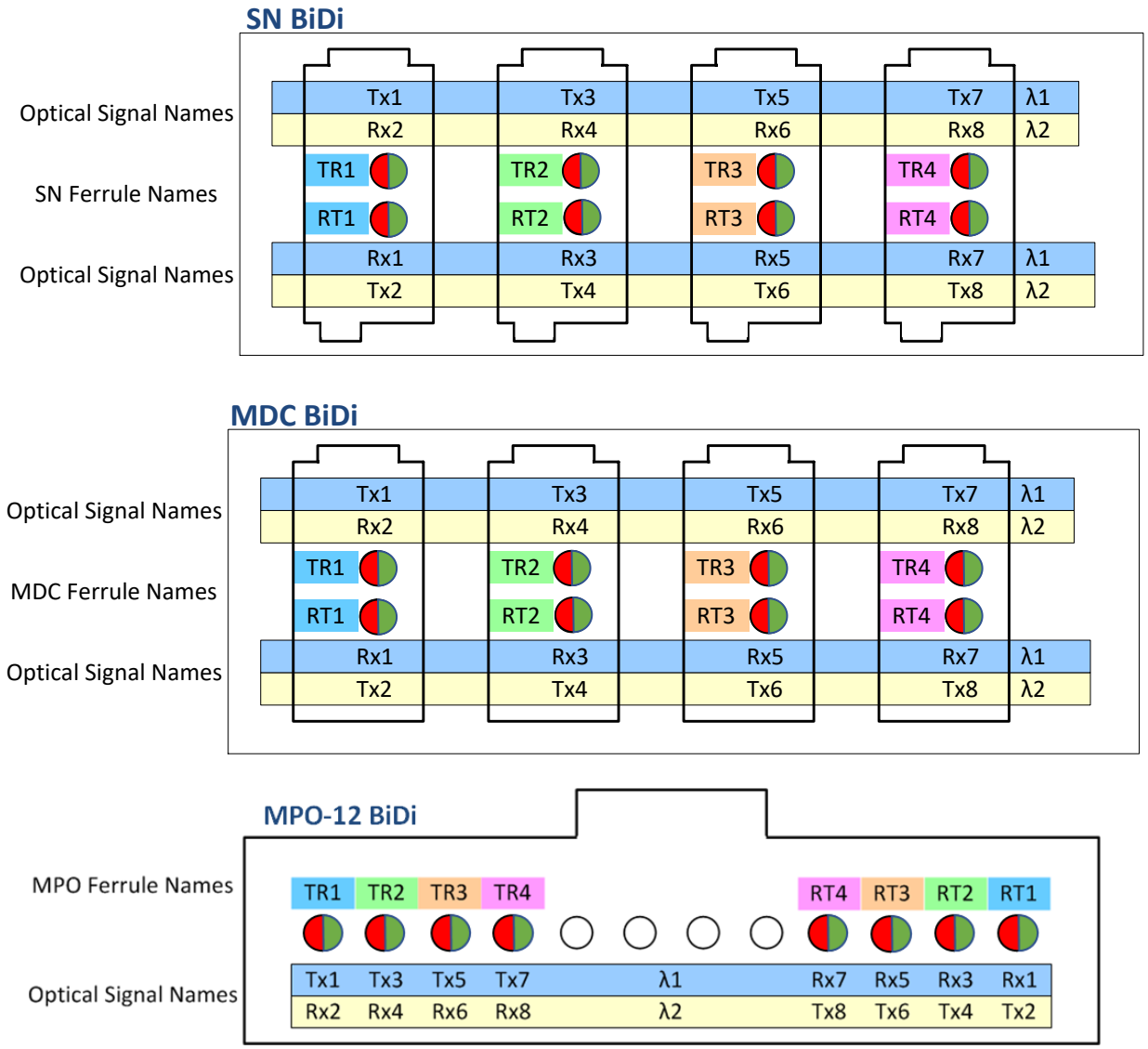












Note: For some CS, SN, and MDC use cases, less connector ports may be needed. In these cases, Port #1 is always the left-most port. Successive ports then follow sequentially from left-to-right as shown.

Figure 14: Optical Media Dependent Interface port assignments

5.2.1 MPO Optical Cable connections

The optical plug and receptacle for the MPO-12 connectors are specified in TIA-604-5 and shown in Figure 15 (MPO-12 Single Row) and Figure 17 (MPO-12 Two Row). The optical plug and receptacle for the MPO-16 connector is specified in TIA-604-18 and shown in Figure 16 (MPO-16 Single Row). Note: This specification uses the terms MPO-12 in place of the TIA term MPO and MPO-12 Two Row in place of the TIA term MPO Two Row.

Aligned keys are used to ensure alignment between the modules and the patchcords. The optical connector is orientated such that the keying feature of the MPO receptacle is on the top. Note: Two alignment pins are present in each receptacle.

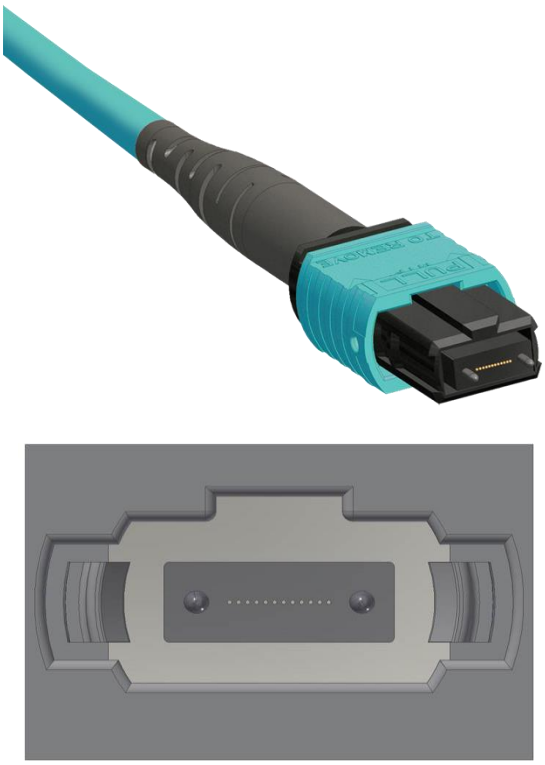


Figure 15: MPO-12 Single Row optical patch cord and module receptacle

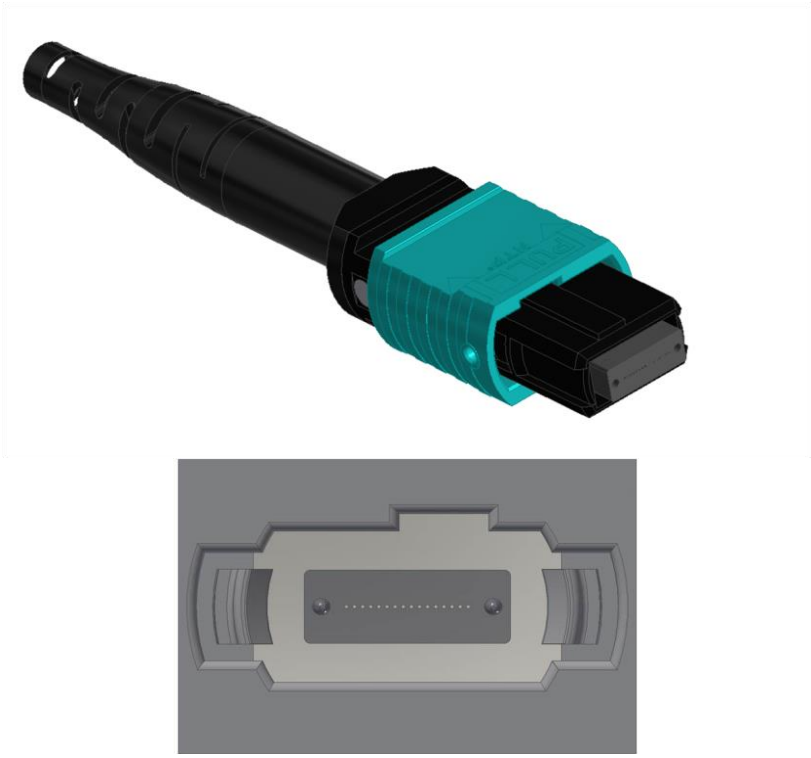


Figure 16: MPO-16 Single Row optical patchcord and module receptacle

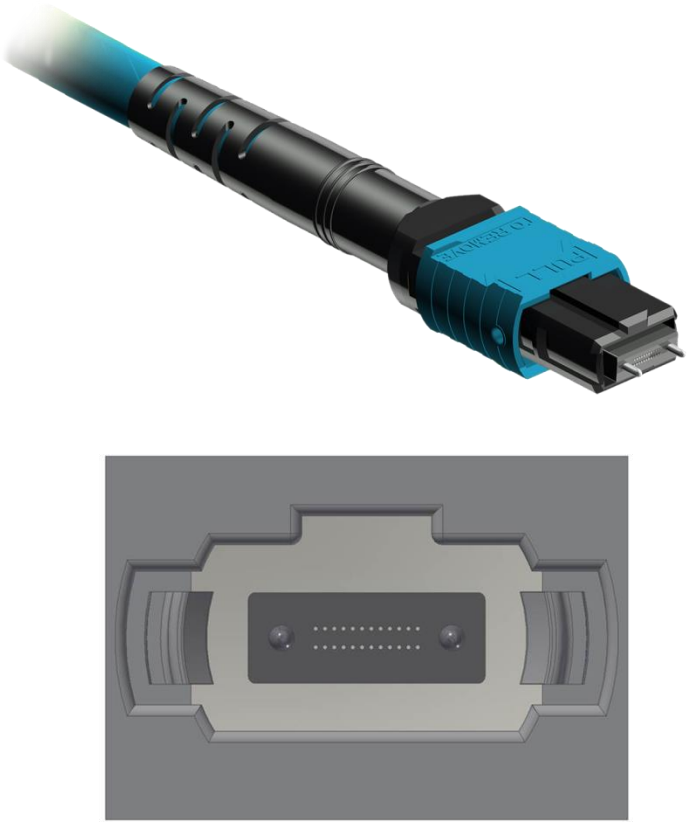


Figure 17: MPO-12 Two Row optical patchcord and module receptacle

5.2.2 Dual LC Optical Cable connection

The Dual LC optical patchcord and module receptacle is specified in TIA-604-10 and shown in Figure 18.

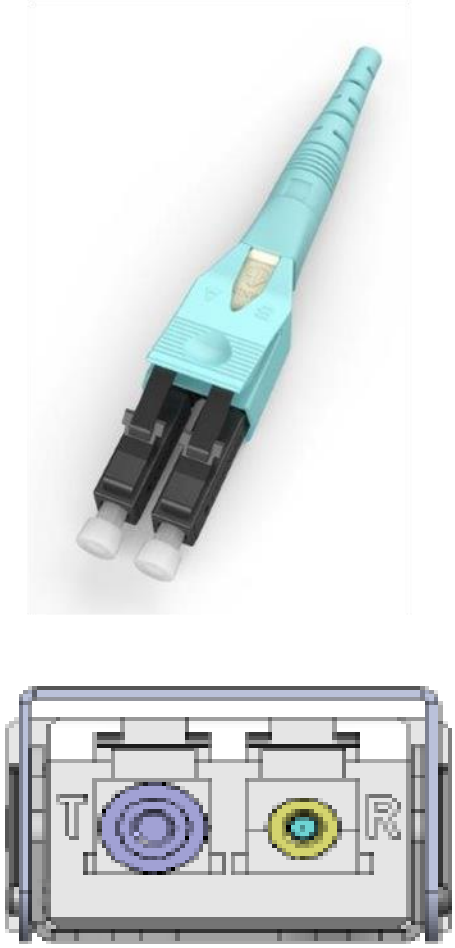


Figure 18: Dual LC optical patchcord and module receptacle

5.2.3 Dual CS Optical Cable connection

The Dual CS optical receptacle for a QSFP-DD module is specified in CS-01242017 and shown in Figure 19.

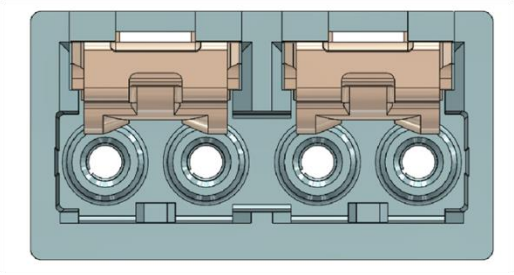


Figure 19: Dual CS connector module receptacle (in support of breakout applications)

5.2.4 SN Quad Optical Cable connections

The SN optical connector and receptacle for QSFP-DD module is specified in SN-60092019 and shown in Figure 20. The top key and offset bottom key are used to ensure alignment between the modules and the patch cords.

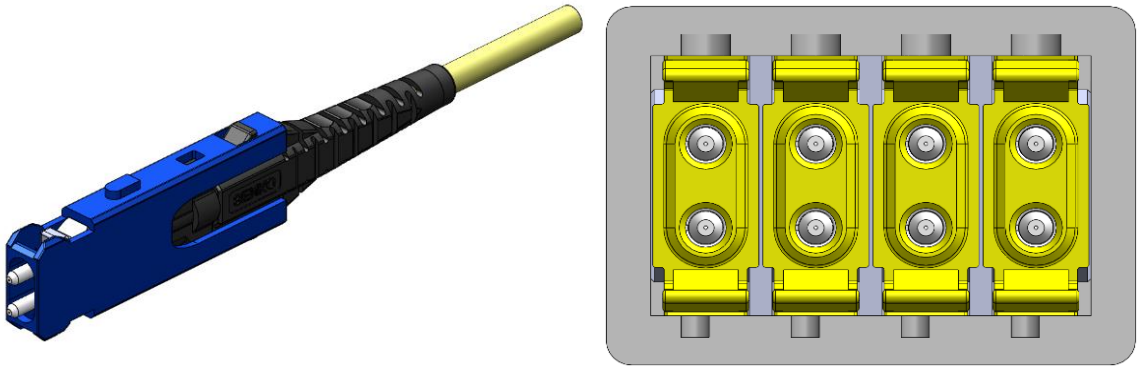


Figure 20: SN quad optical connector plug and four-port module receptacle

5.2.5 MDC Quad Optical Cable connection

The MDC optical plug and receptacle for a QSFP-DD module is specified in USC-11383001 and shown in Figure 21. The optical connector is orientated such that the keying feature of the MDC receptacle is on the top.

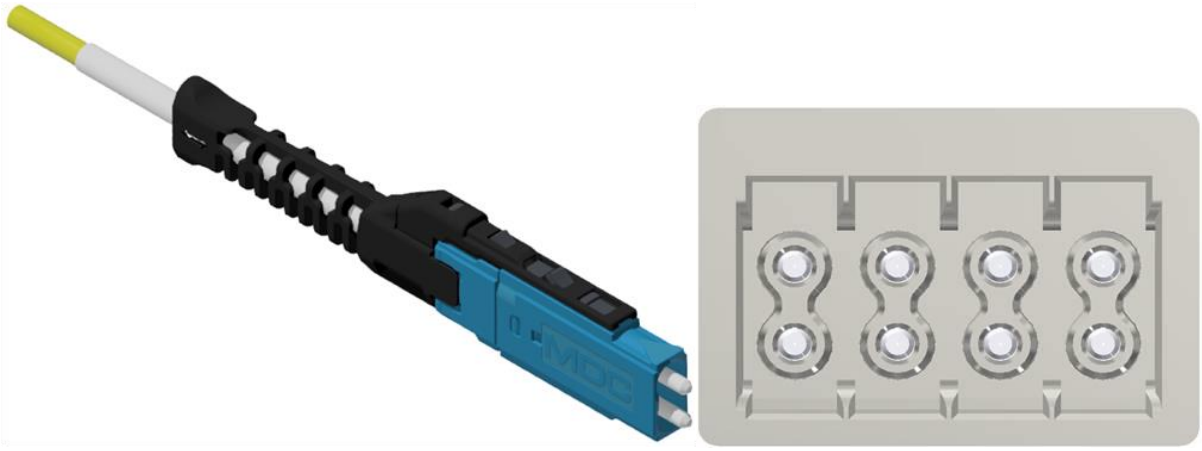


Figure 21: MDC quad optical connector plug and four-port module receptacle

5.2.6 SN Dual Optical Cable connections

The SN optical connector and receptacle for QSFP-DD module is specified in SN-60092019 and shown in Figure 22. The top key and offset bottom key are used to ensure alignment between the modules and the patch cords.

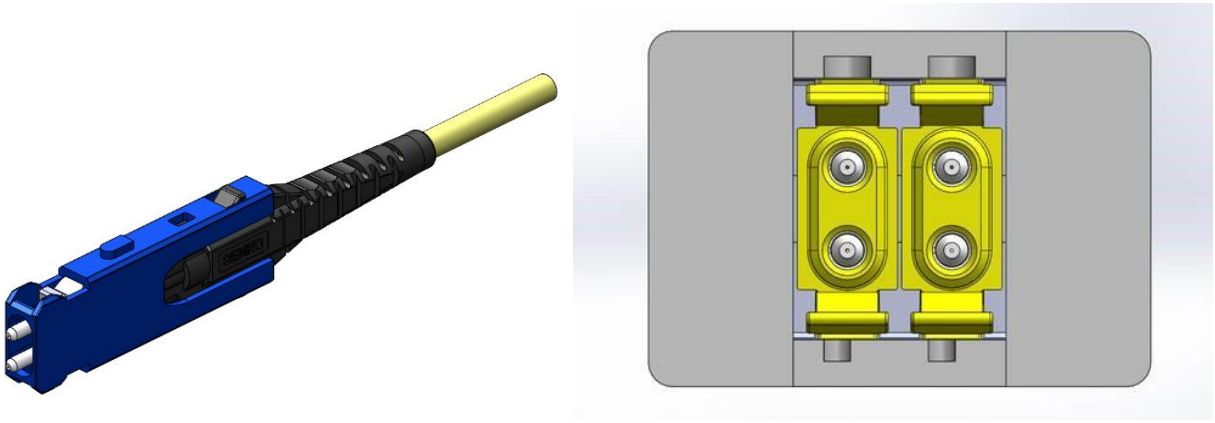


Figure 22: SN dual optical connector plug and four-port module receptacle

5.2.7 MDC dual Optical Cable connection

The MDC dual optical plug and receptacle for a QSFP-DD module is specified in USC-11383001 and shown in Figure 23. The optical connector is orientated such that the keying feature of the MDC receptacle is on the top.

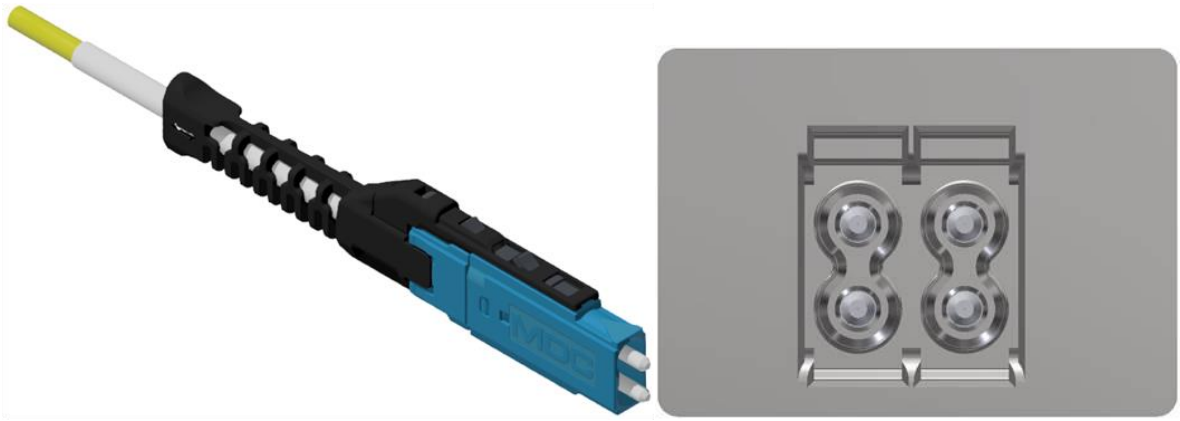


Figure 23: MDC dual optical connector plug and four-port module receptacle

5.3 Module Color Coding and Labeling

An exposed feature of the QSFP-DD module (a feature or surface extending outside of the bezel) shall be color coded as follows:

Beige for 850nm
Blue for 1310nm
White for 1550nm

Each QSFP-DD module shall be clearly labeled. The complete labeling need not be visible when the QSFP-DD module is installed and the bottom of the device is the recommended location for the label. Labeling shall include:

Appropriate manufacturing and part number identification
Appropriate regulatory compliance labeling
A manufacturing traceability code

The label should also include clear specification of the external port characteristics such as:

Optical wavelength
Required fiber characteristics (i.e. MMF/SMF)
Operating data rate
Interface standards supported
Link length supported
Connector Type

If required to comply with 7.3, a label must be applied to the top external surface of the module case, warning of high touch temperature.

The labeling shall not interfere with the mechanical, thermal or EMI features.

6 Mechanical and Board Definition

6.1 Introduction

The cages and modules defined in this chapter are illustrated in Figure 24 (2x1 stacked cage and module), Figure 25 (press fit cage for surface mount connector}, Figure 26 (Type 1 pluggable module) and Figure 27 (Type 2 pluggable module). All pluggable modules and direct attach cable plugs (both Type 1 and Type 2) must mate to the connectors and cages defined in this specification. The Type 2 module allows an additional extension of the module outside of the cage to allow for flexibility in module design. A Type 2A module includes a heat sink on the extension of the module outside the cage to provide enhanced thermal performance. Heat sink/clip thermal designs are application specific and not specifically defined by this specification. See Appendix A for informative recommendations on overall module length including handle. See Appendix B for recommended heat sink design for Type 2A modules.

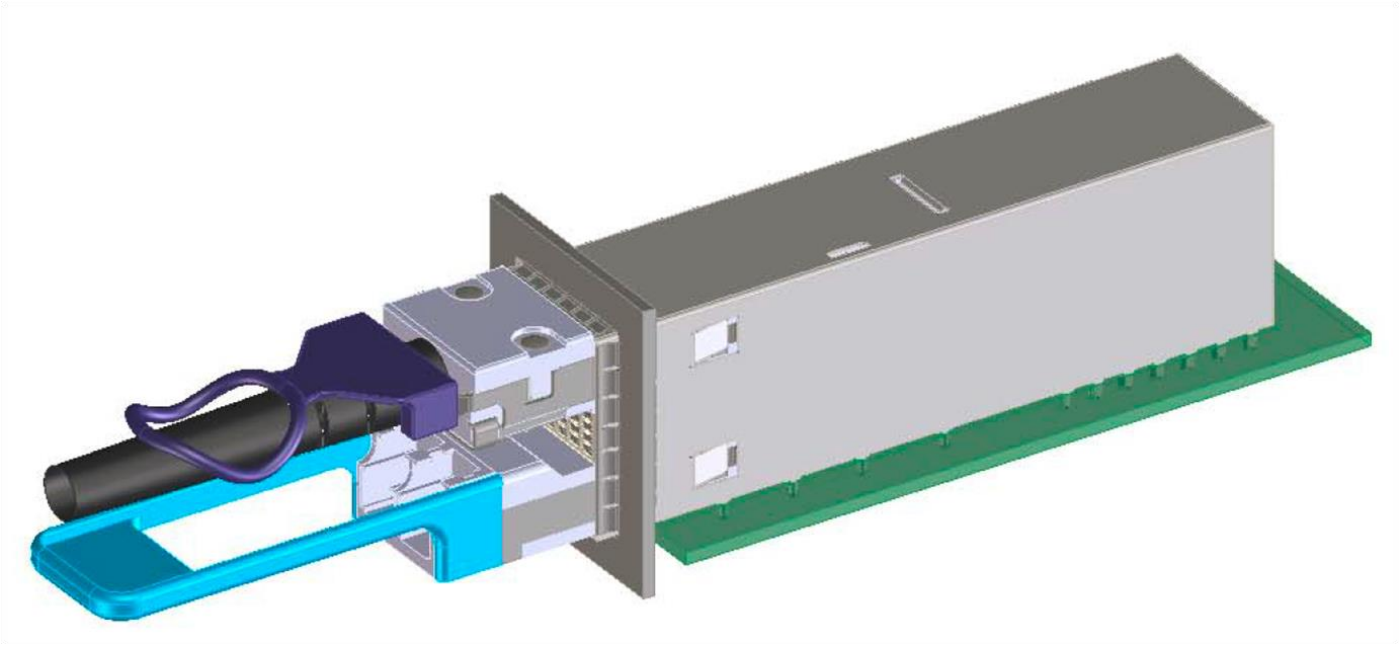


Figure 24: 2x1 stacked cage and module

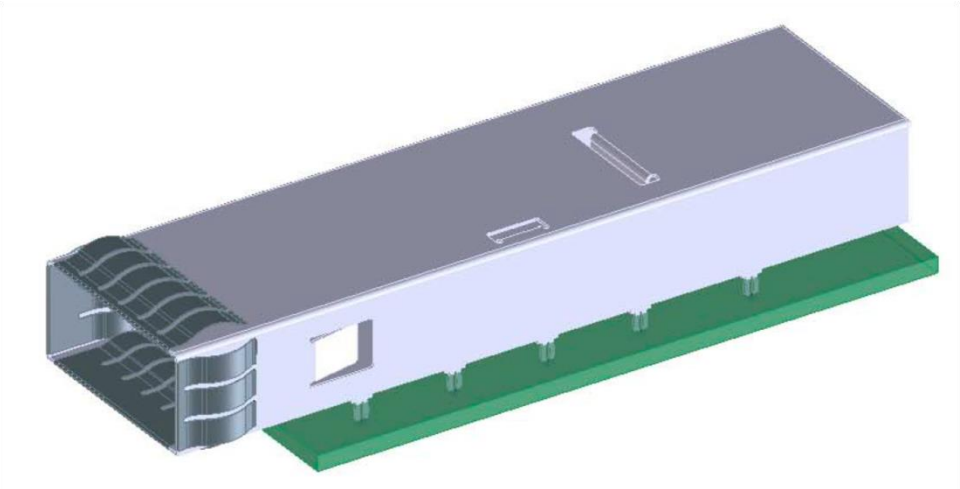


Figure 25: Press fit cage for surface mount (SMT) connector

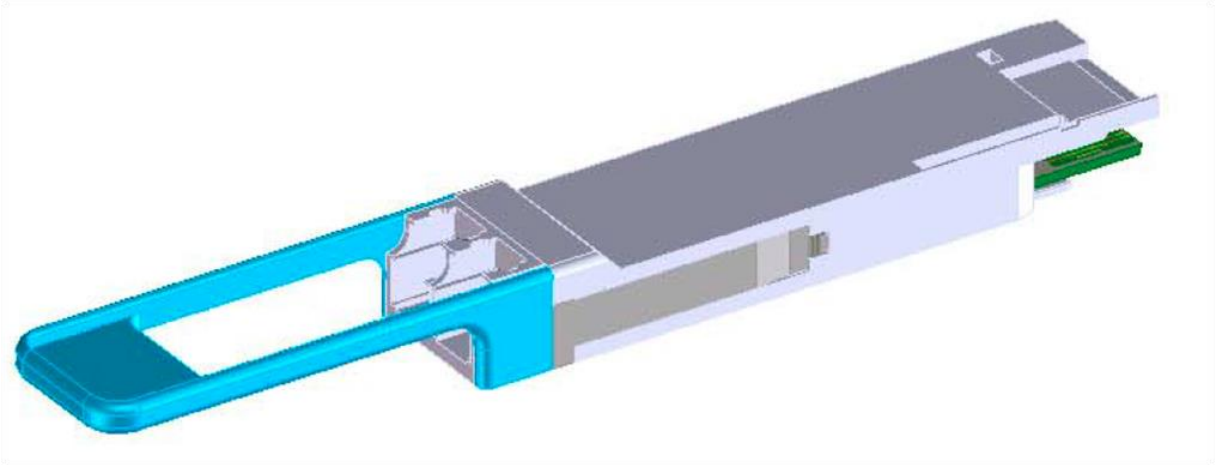


Figure 26: Type 1 Pluggable module

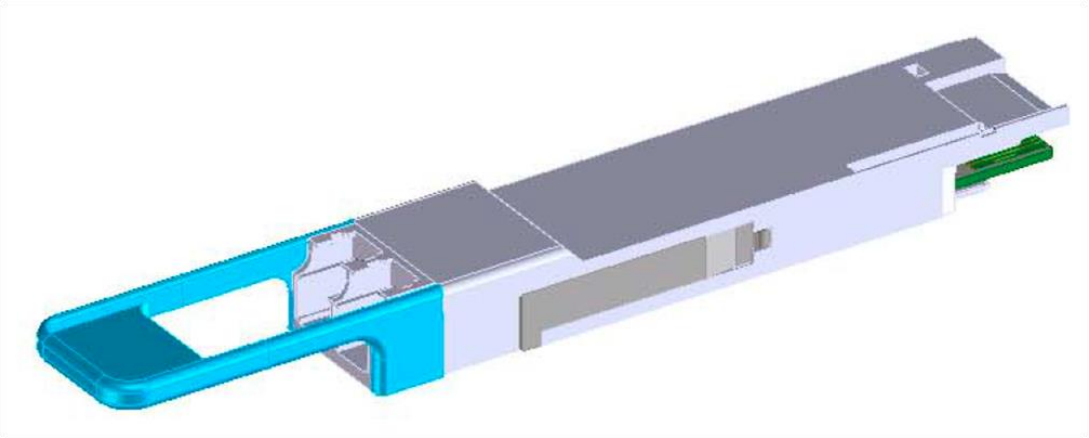


Figure 27: Type 2 Pluggable module

6.2 Datums, Dimensions and Component Alignment

A listing of the datums for the various components is contained in Table 10. The alignments of some of the datums are noted. In order to reduce the complexity of the drawings, all dimensions are considered centered unless otherwise specified. Dimensions and tolerancing conform to ASME Y14.5-2009. All dimensions are in millimeters.

Table 10- Datums

Datum[1]	Description
A	Host Board Top Surface
B	Inside surface of bezel
C	Distance between Connector terminal thru holes on host board[3]
D	Hard stop on module[2]
E	Width of module[3]
F	Height of module housing
G	Width of module pc board[3]
H	Leading edge of signal contact pads on module pc board
J	Top surface of module pc board
K	Host board thru hole #1 to accept connector guidepost[2]
L	Host board thru hole #2 to accept connector guidepost[2]
M	Width of bezel cut out[3]
P	Vertical Center line of internal surface of cage
S	Seating plane of cage on host board
T	Hard stop on cage[2]
AA	Connector slot width[3]
BB	Seating plane of connector on host board
DD	Top surface of module housing
EE	Centerline of module opening to locate paddle card Datum H
FF	Centerline of upper port cage height
GG	Centerline of lower port cage height
EE	Primary Datum hole for 2x1 Host PCB

Notes:
1. All dimensions are in mm.
2. Datums D and T are aligned when assembled (see Figure 28 and Figure 29).
3. Centerlines of datums AA, C, E, G, M are aligned on the same vertical plane.

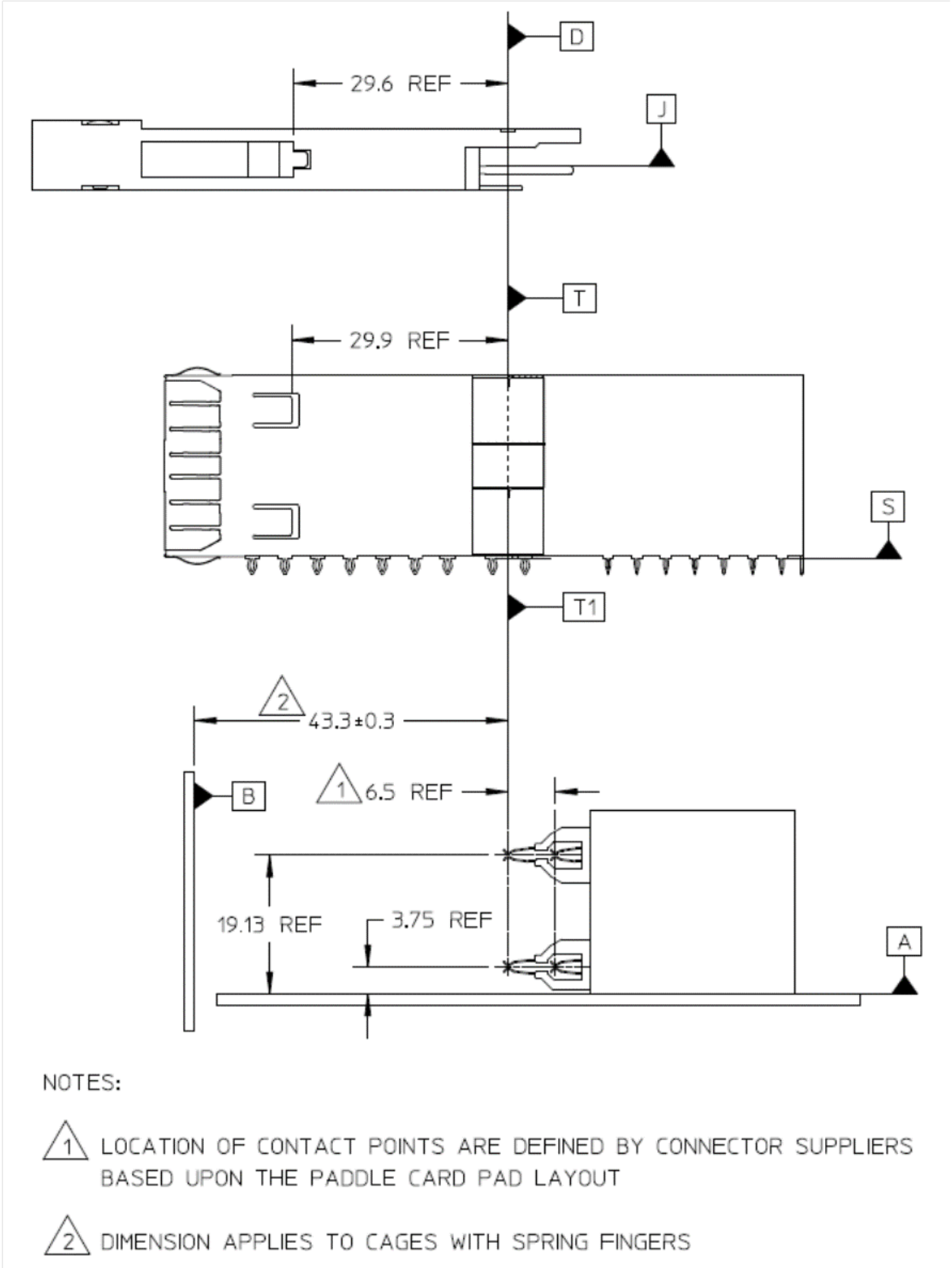


Figure 28: 2X1 stacked connector/cage datum descriptions

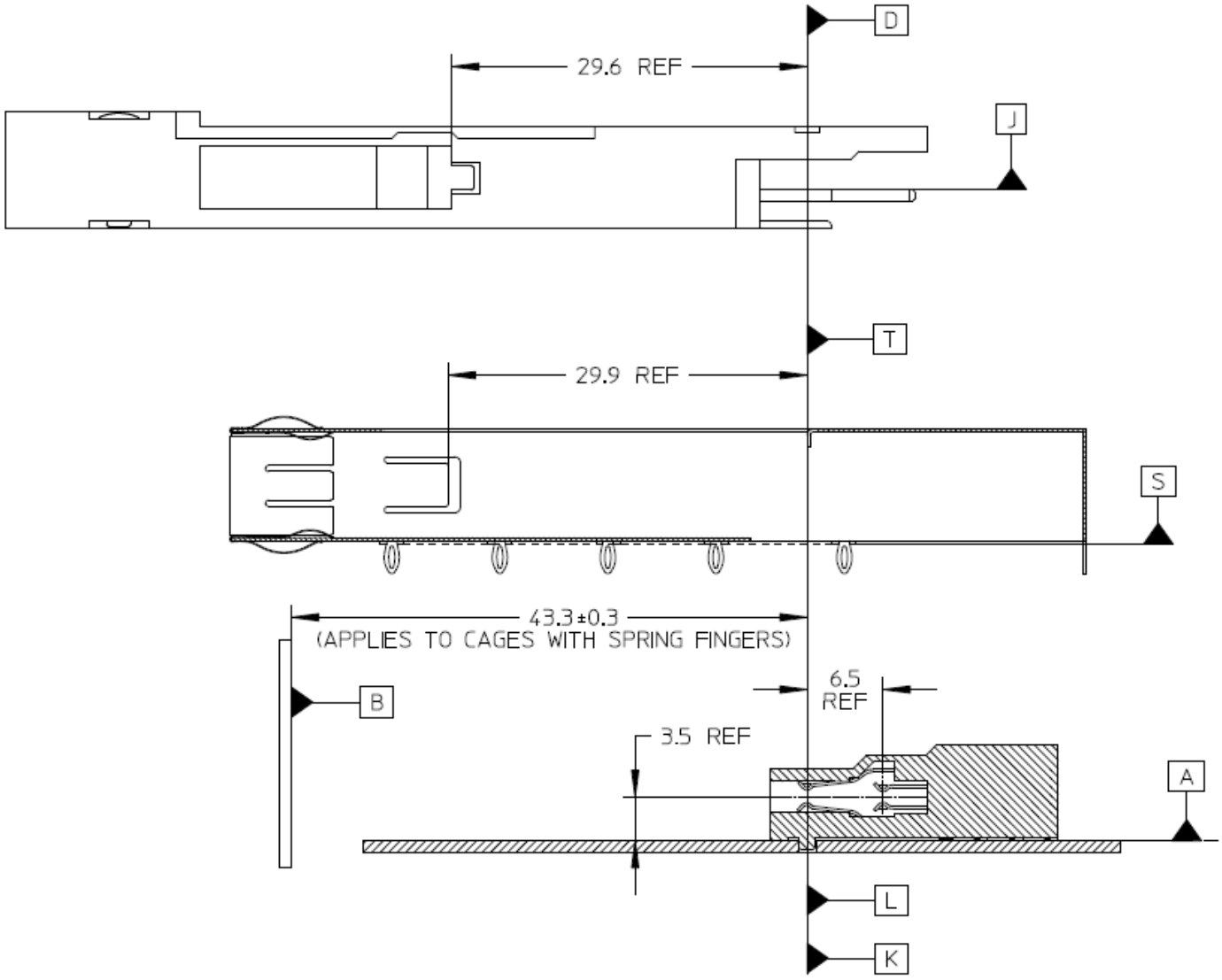


Figure 29: Surface mount connector/cage datum descriptions

6.3 Module Mechanical Dimensions

The mechanical outline for the Type 1 module is shown in Figure 30, the Type 2 module is shown in Figure 31 and the Type 2A module in Figure 32. The module shall provide a means to self-lock with either the 2x1 stacked cage or SMT cage upon insertion. The module package dimensions are defined in Figure 33 and Figure 35. The dimensions that control the size of the module that extends outside of the cage are listed as maximum dimensions per Note 4 in Figure 33.

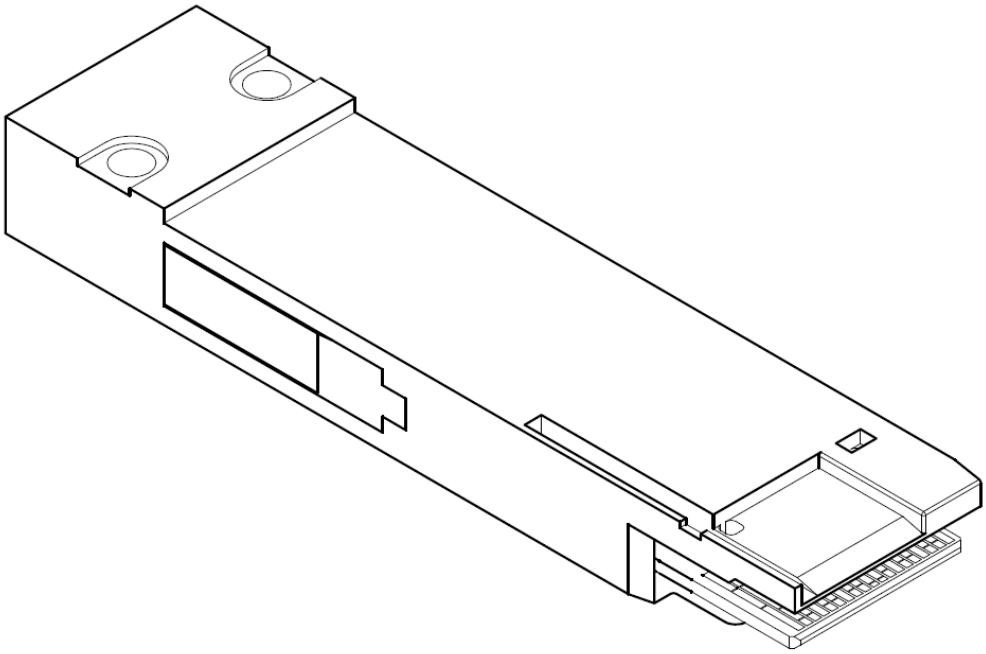


Figure 30: Type 1 Module

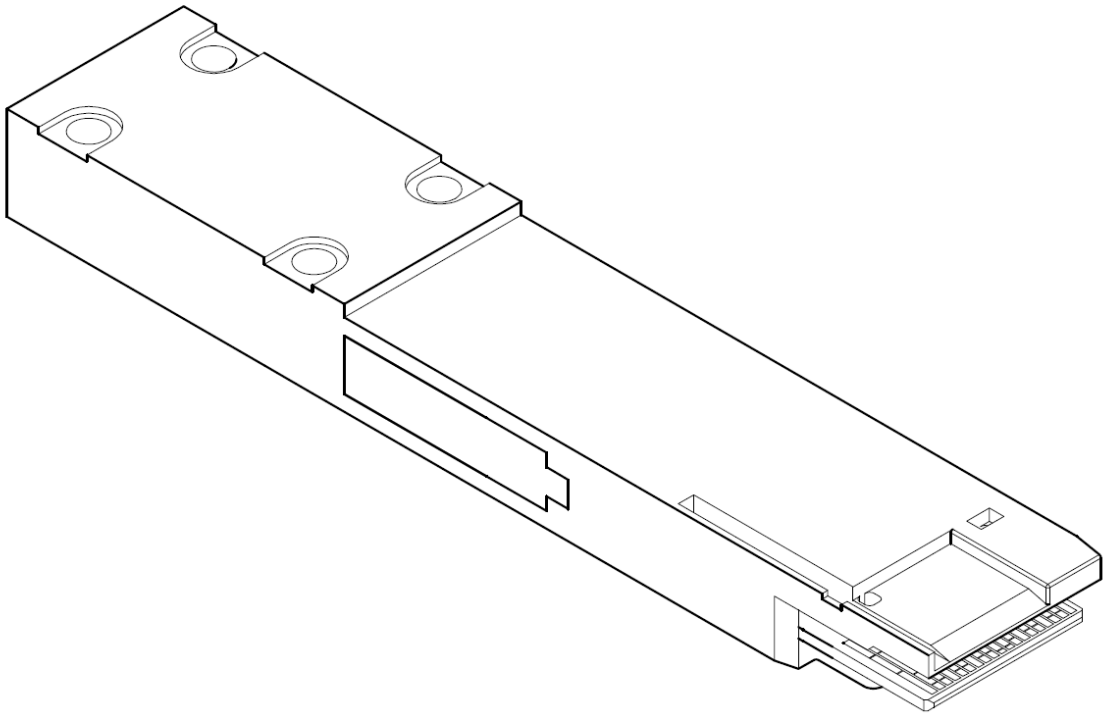


Figure 31: Type 2 Module

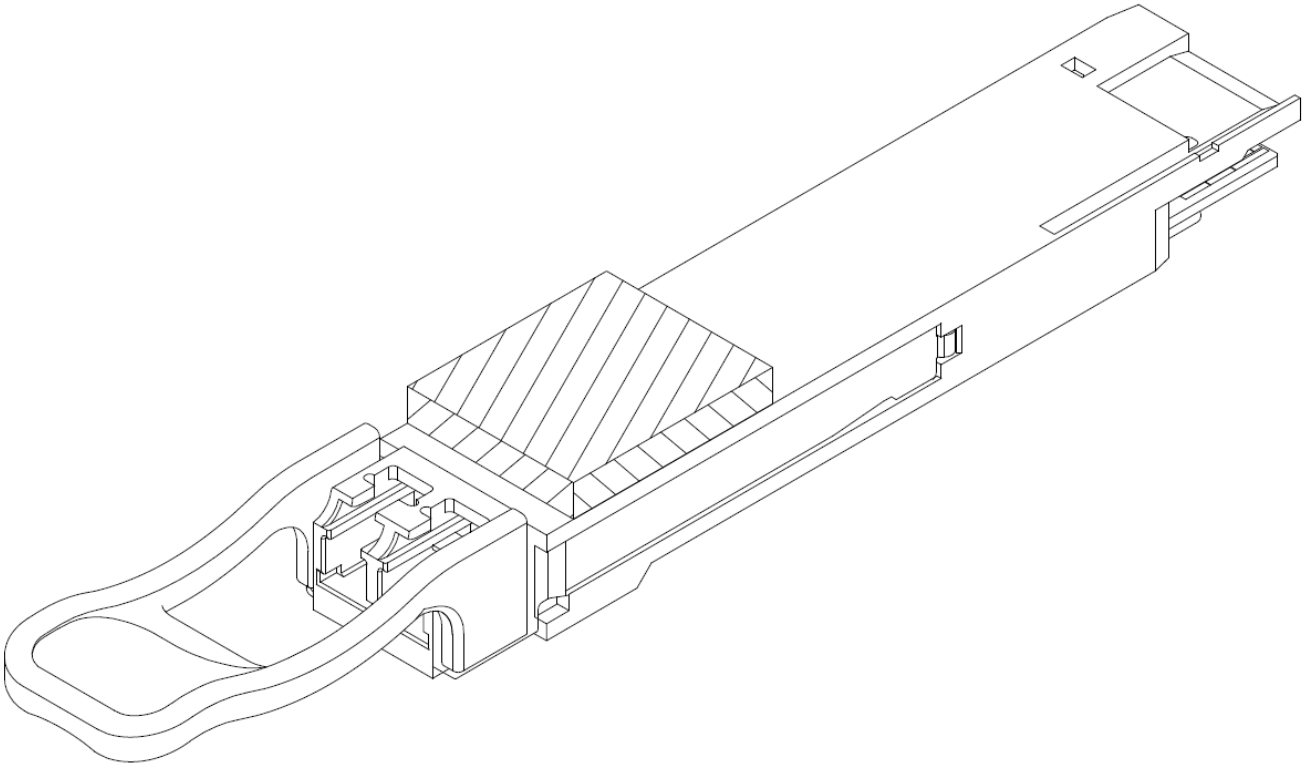


Figure 32: Type 2A Module

NOTES APPLY TO MODULE DRAWING

1. DIMENSIONS AND TOLERANCING CONFORM TO ASME Y14.5-2009.
2. ALL DIMENSIONS ARE IN MILLIMETERS.
3. UNLESS OTHERWISE SPECIFIED, SHARP CORNERS AND EDGES ARE NOT ALLOWED. ROUND OFF ALL EDGES AND CORNERS TO A MINIMUM RADIUS OF 0.10 MM.

4 DIMENSION DEFINES ENLARGED SECTION OF TRANSCEIVER THAT EXTENDS OUTSIDE OF CAGE TO ACCOMMODATE MATING PLUG AND ACTUATOR MECHANISM.

5 SURFACES ON ALL 4 SIDES OF THE 12.4 MIN DIMENSION TO BE CONDUCTIVE FOR CONNECTION TO CHASSIS GROUND.

6 DIMENSION APPLES TO LATCH MECHANISM.

7 DIMENSION APPLIES TO THE LOCATION OF THE EDGE OF THE MODULE BOARD PAD, DATUM H. CONTACTS 21, 22, 36 AND 37 ARE VISIBLE.

8 DIMENSION TO INCLUDE BAIL TRAVEL.

9 DIMENSION APPLY TO OPENINGS IN THE HOUSING.

10 OPTIONAL FEATURE TO AID INSPECTION OF DIMENSIONS FROM DATUM D.

11 FLATNESS AND SURFACE ROUGHNESS (Ra) APPLIES FOR INDICATED LENGTH AND MIN WIDTH OF 13MM. SURFACE TO BE THERMALLY CONDUCTIVE. SEE SECTION 5.4 TABLE 8 FOR FLATNESS AND ROUGHNESS REQUIREMENTS.

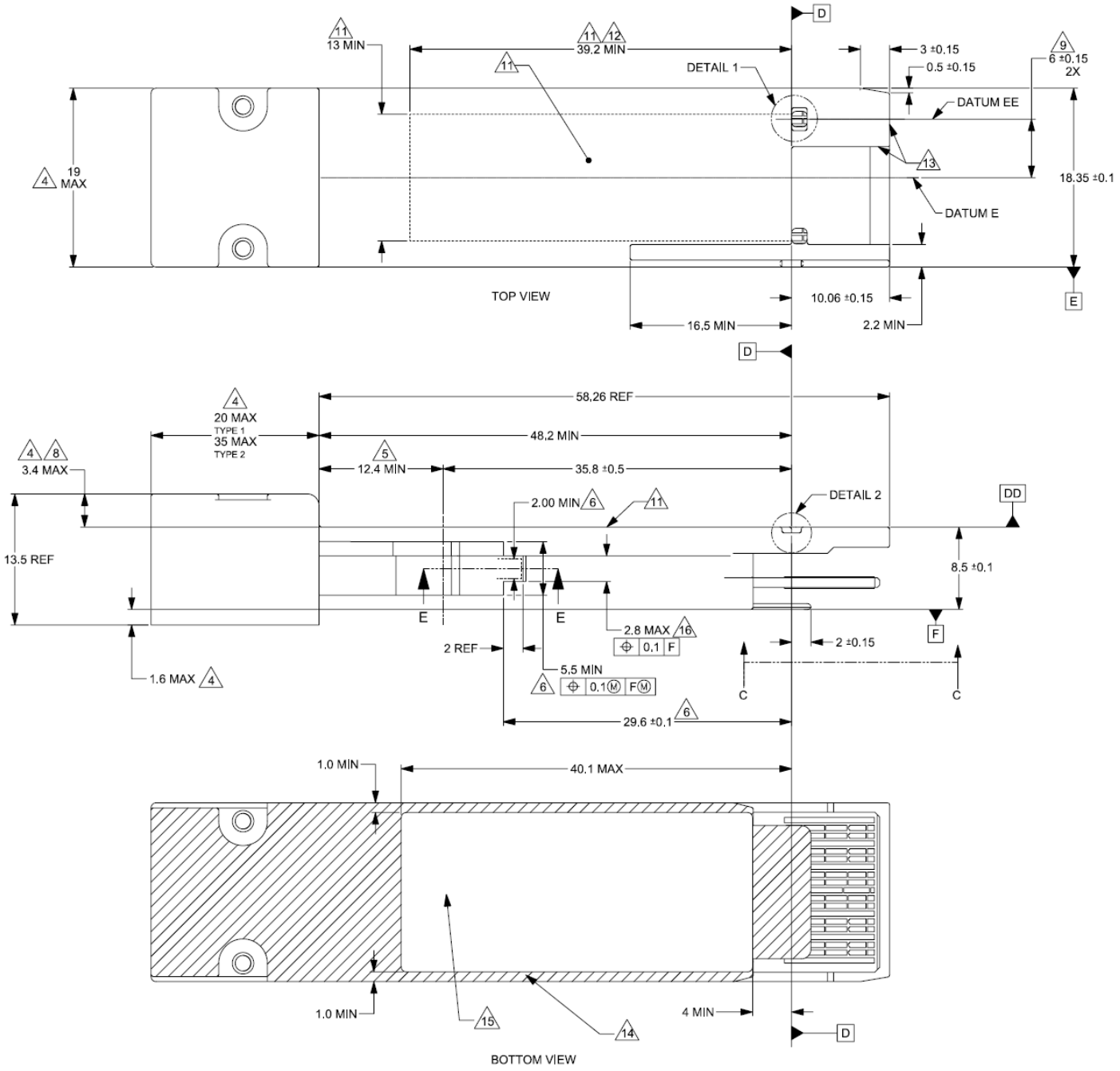
12 HIGHER WATTAGE MODULES MAY REQUIRE ADDITIONAL SPACE FOR COOLING.

13 BLOCKING FEATURE IS CRITICAL TO APPLICATION FUNCTION. A RADIUS OF 0.1 ± 0.05 MM IS REQUIRED ON THE LEADING EDGES OF THIS FEATURE.

14 LABELS PERMITTED ON BOTTOM OF MODULE. LABEL TO BE ZERO THICKNESS OR RECESSED BELOW BOTTOM SURFACE OF MODULE. LABEL CONTENTS AND POSITION TO BE DETERMINED BY MODULE MANUFACTURER BUT ARE NOT ALLOWED IN THE KEEP OUT AREA SHOWN IN THE BOTTOM VIEW.

15 THE LABEL(S) SHALL NOT INTERFERE WITH THE MECHANICAL, THERMAL, OR EMI PROPERTIES AND MUST NOT VIOLATE NOTE 5.

16 DIMENSION APPLIES TO LATCH POCKET


11
13 MIN
11 12
39.2 MIN
11
DETAIL 1
D
3 ±0.15
0.5 ±0.15
9
6 ±0.15
2X
DATUM EE
13
18.35 ±0.1
4
19
MAX
DATUM E
TOP VIEW
10.06 ±0.15
E
16.5 MIN
2.2 MIN
D
4
20 MAX
TYPE 1
35 MAX
TYPE 2
58.26 REF
48.2 MIN
4 8
3.4 MAX
5
12.4 MIN
35.8 ±0.5
2.00 MIN 6
11
DETAIL 2
DD
13.5 REF
8.5 ±0.1
E
E
2.8 MAX 16
0.1 F
F
2 ±0.15
2 REF
5.5 MIN
6
0.1 M F M
C
C
1.6 MAX 4
6
29.6 ±0.1
1.0 MIN
40.1 MAX
1.0 MIN
15
14
4 MIN
D
BOTTOM VIEW

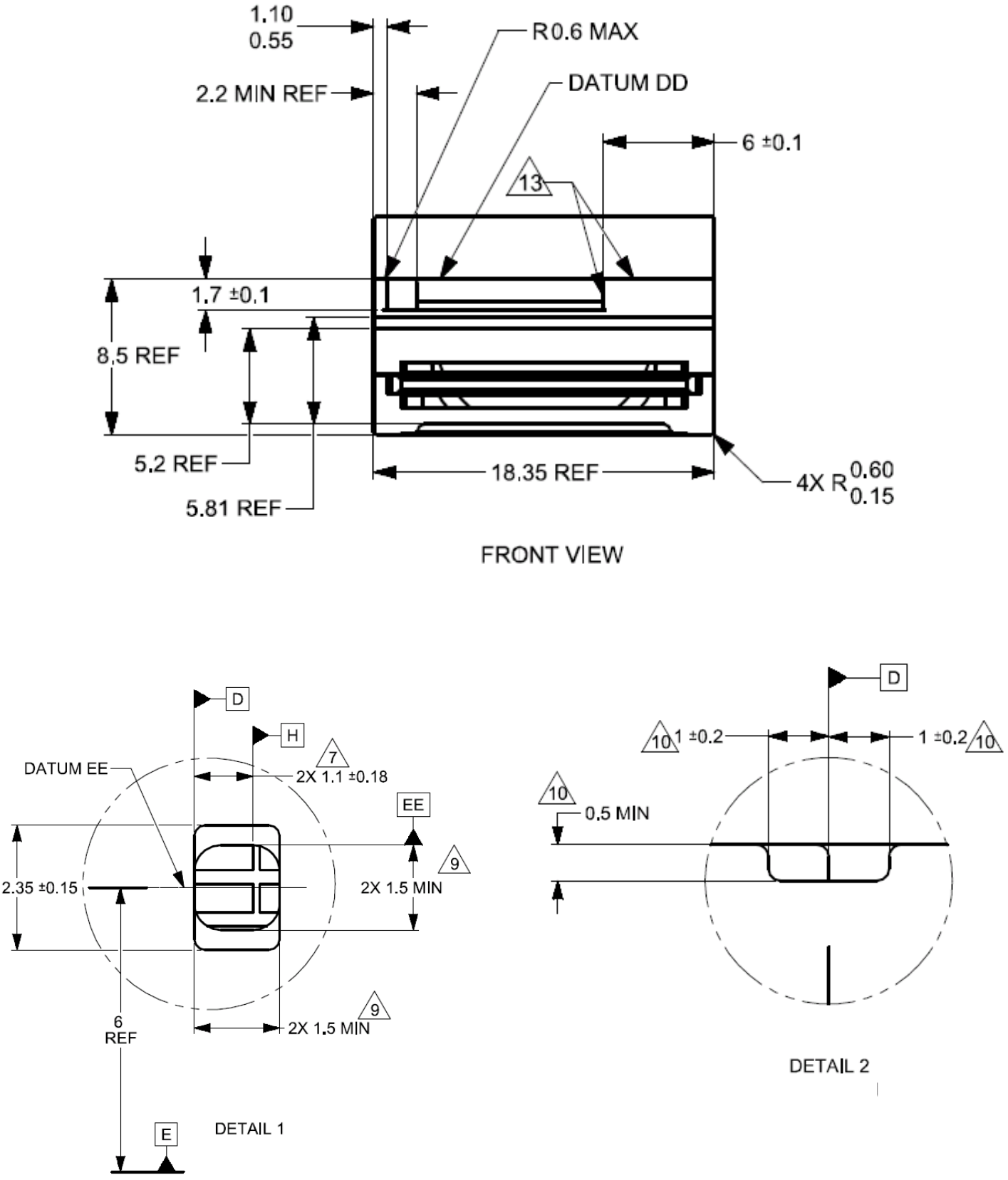


Figure 33: Drawing of module

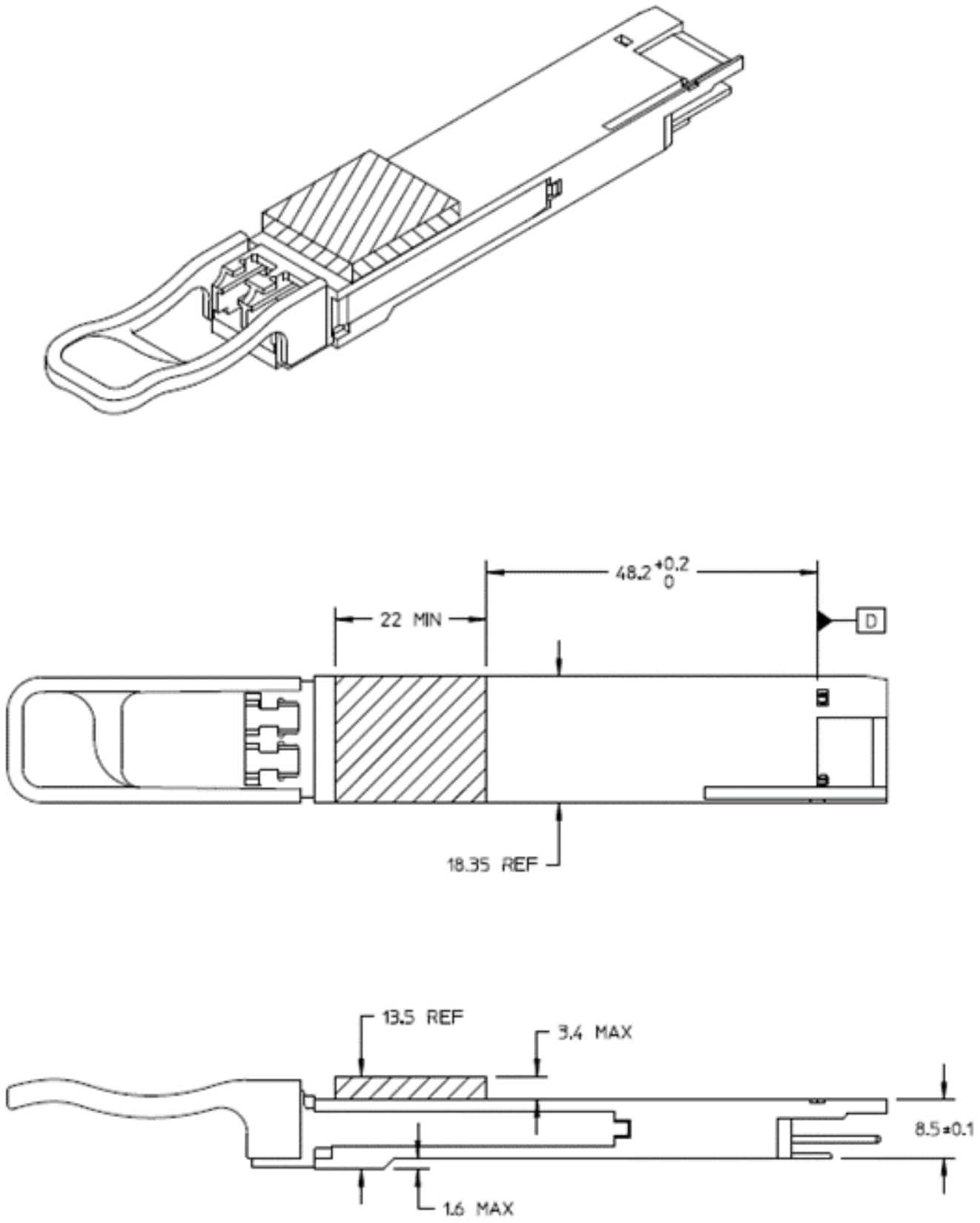
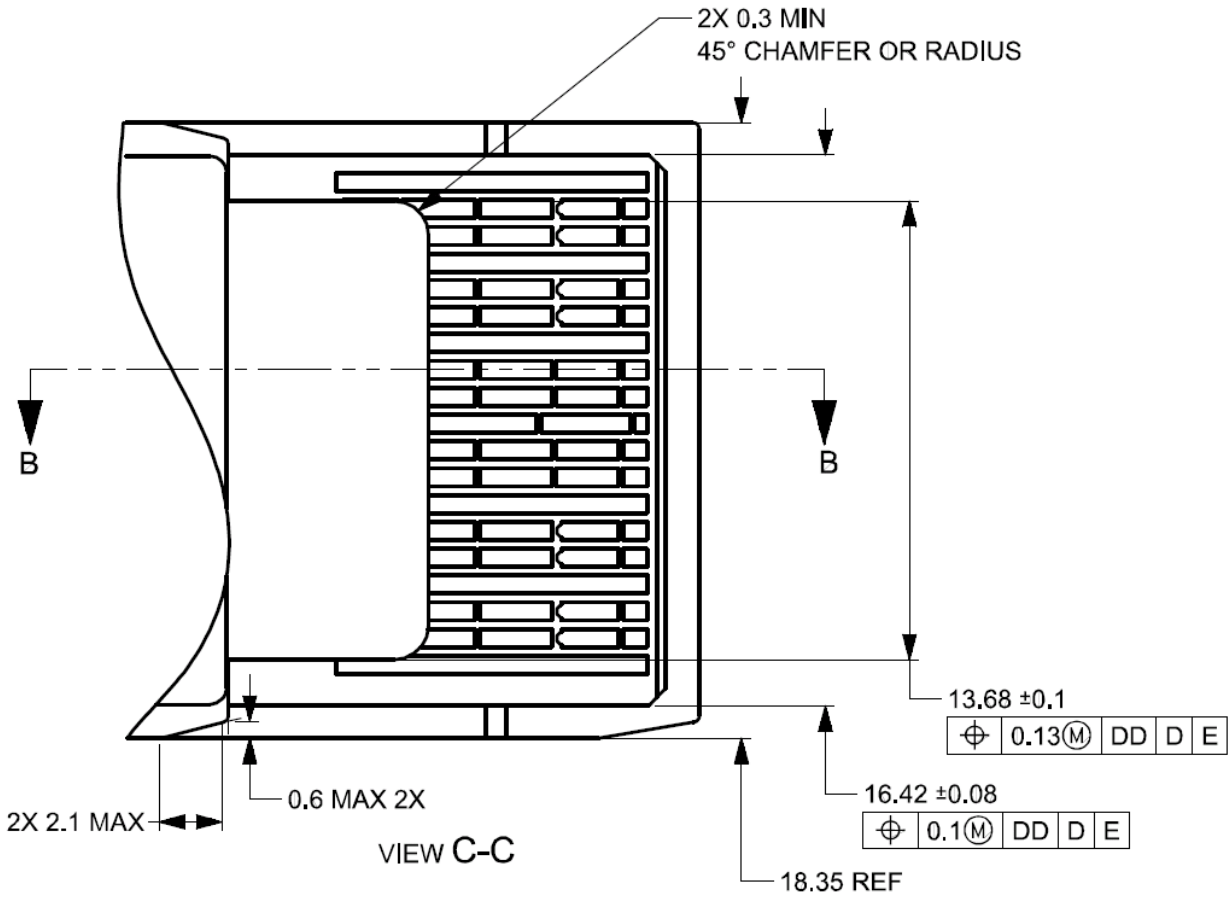


Figure 34: Type 2A Module with Heat Sink


2X 0.3 MIN
45° CHAMFER OR RADIUS
B
B
13.68 ±0.1
0.13 M DD D E
16.42 ±0.08
0.1 M DD D E
18.35 REF
0.6 MAX 2X
2X 2.1 MAX
VIEW C-C

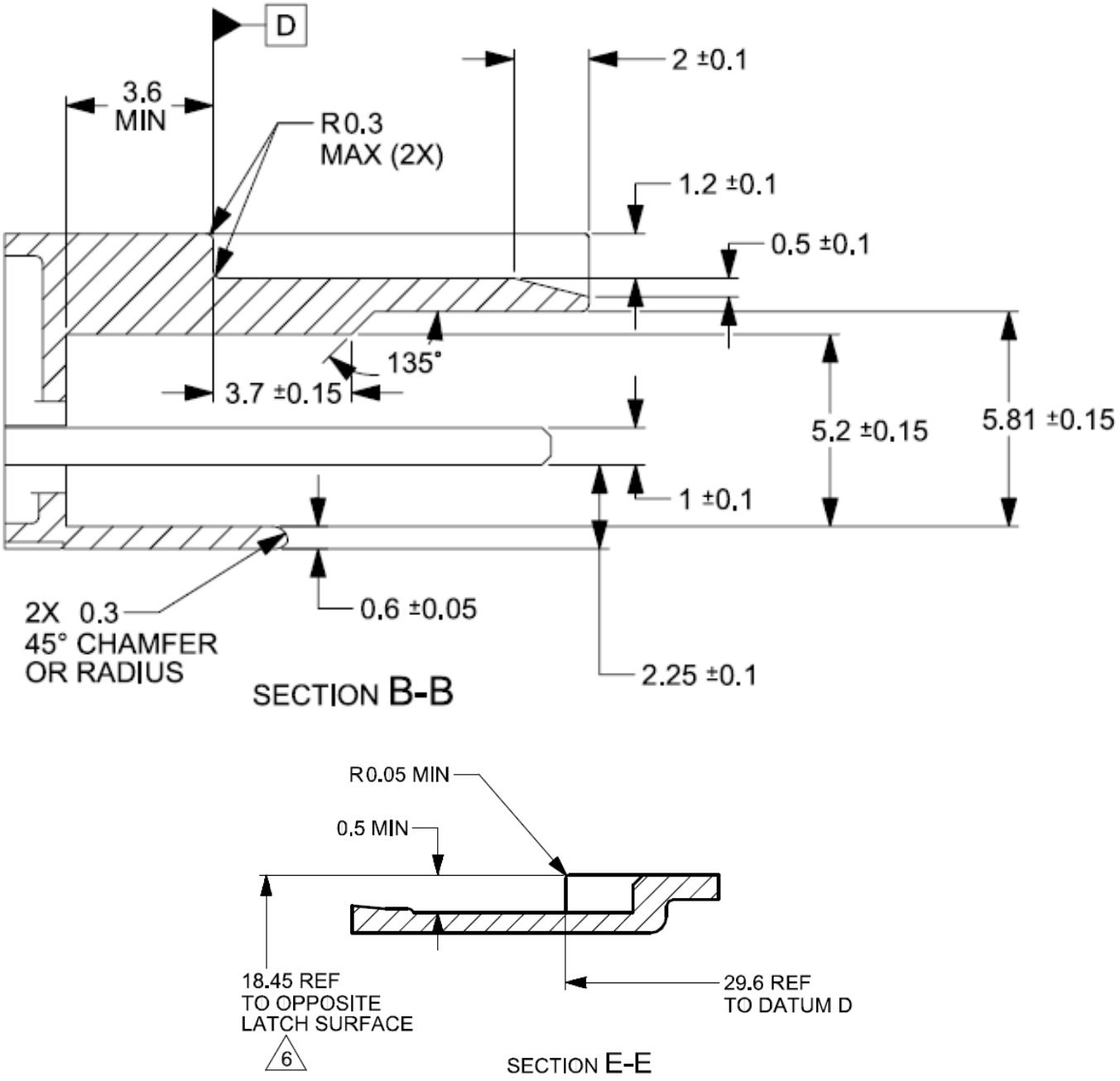


Figure 35: Detailed dimensions of module

6.4 Module Flatness and Roughness

Module flatness and roughness are specified to improve module thermal characteristics when used with a riding heat sink. Relaxed specifications are used for lower power modules to reduce cost. The module flatness and roughness specifications apply to the specified heat sink contact area as specified in Figure 33. Specifications for Module flatness and surface roughness are shown in Table 11 (see Figure 33 note 11).

Table 11- Module flatness specifications

Power Class	Module Flatness (mm)	Surface Roughness (Ra,µm)
1	0.075	1.6
2	0.075	1.6
3	0.075	1.6
4	0.075	1.6
5	0.050	0.8
6	0.050	0.8
7	0.050	0.8
8	0.050	0.8

6.5 Module paddle card dimensions notes

Notes for module paddle cards drawings applies to Figure 36 and Figure 37.

1. DIMENSIONING AND TOLERANCING CONFORM TO ASME Y14.5-2009
2. ALL DIMENSIONS ARE IN MILLIMETERS
3. NO SOLDER MASK WITHIN 0.05 MM OF ALL DEFINED CONTACT PAD EDGES
4. NO SOLDER MASK BETWEEN END CONTACTS AND THE SIDES OF THE PADDLE CARD

△5 DATUM H IS ESTABLISHED WITH DATUM TARGET POINTS AT THE LEADING EDGE OF THE OUTER MOST SIGNAL CONTACTS PADS TO BE RE-ESTABLISHED ON EACH SIDE

△6 DIMENSION APPLIES FROM THE FIRST SET OF SIGNAL PADS TO THE SECOND SET OF SIGNAL PADS

△7 DIMENSION AND TOLERANCE APPLIES TO ALL GROUND PADS ON BOTH TOP AND BOTTOM SIDE OF PADDLE CARD

△8 DIMENSION AND TOLERANCE APPLIES TO ALL POWER PADS ON BOTH TOP AND BOTTOM SIDE OF PADDLE CARD

△9 DIMENSION AND TOLERANCE APPLIES TO ALL SIGNAL PADS ON BOTH TOP AND BOTTOM SIDE OF PADDLE CARD

△10 A ZERO GAP IS ALLOWED FOR A CONTINUOUS PAD OPTION

△11 APPLIES TO ALL SIGNAL PAD TO PAD SPACING

△12 PRE-WIPE PADS (SHADED AREA) ON MODULE CARD HOST SIDE ARE OPTIONAL

△13 PRE-WIPE PADS (UNSHADED AREA) ARE REQUIRED EXCEPT IN CONTINUOUS POWER OR GROUND PAD DESIGNS

△14 PADDLE CARD THICKNESS IS MEASURED OVER PADS VIAS MUST NOT BE PROUD OF THE PAD SURFACE

△15 MINIMUM DIMENSION REQUIRED FOR MATING SEQUENCE BETWEEN SIGNAL AND GROUND PADS

△16 MINIMUM DIMENSION REQUIRED FOR MATING SEQUENCE BETWEEN SIGNAL AND POWER PADS

△17 COMPONENT KEEP OUT AREA MEASURED FROM DATUM H

△18 A SINGLE SPLIT IN THE PRE-WIPE SIGNAL PAD IS OPTIONAL, AND IF IMPLEMENTED, THE RESULTING 2 PADS SHALL BE SEPARATED WITH A GAP OF 0.13 ± 0.05

19. CONTACT PAD PLATING
    0.38 MICROMETERS MINIMUM GOLD OVER
    1.27 MICROMETERS MINIMUM NICKEL
    ALTERNATE CONTACT PAD PLATING
    0.05 MICROMETERS MINIMUM GOLD OVER
    0.30 MICROMETERS MINIMUM PALLADIUM OVER
    1,27 MICROMETERS MINIMUM NICKEL

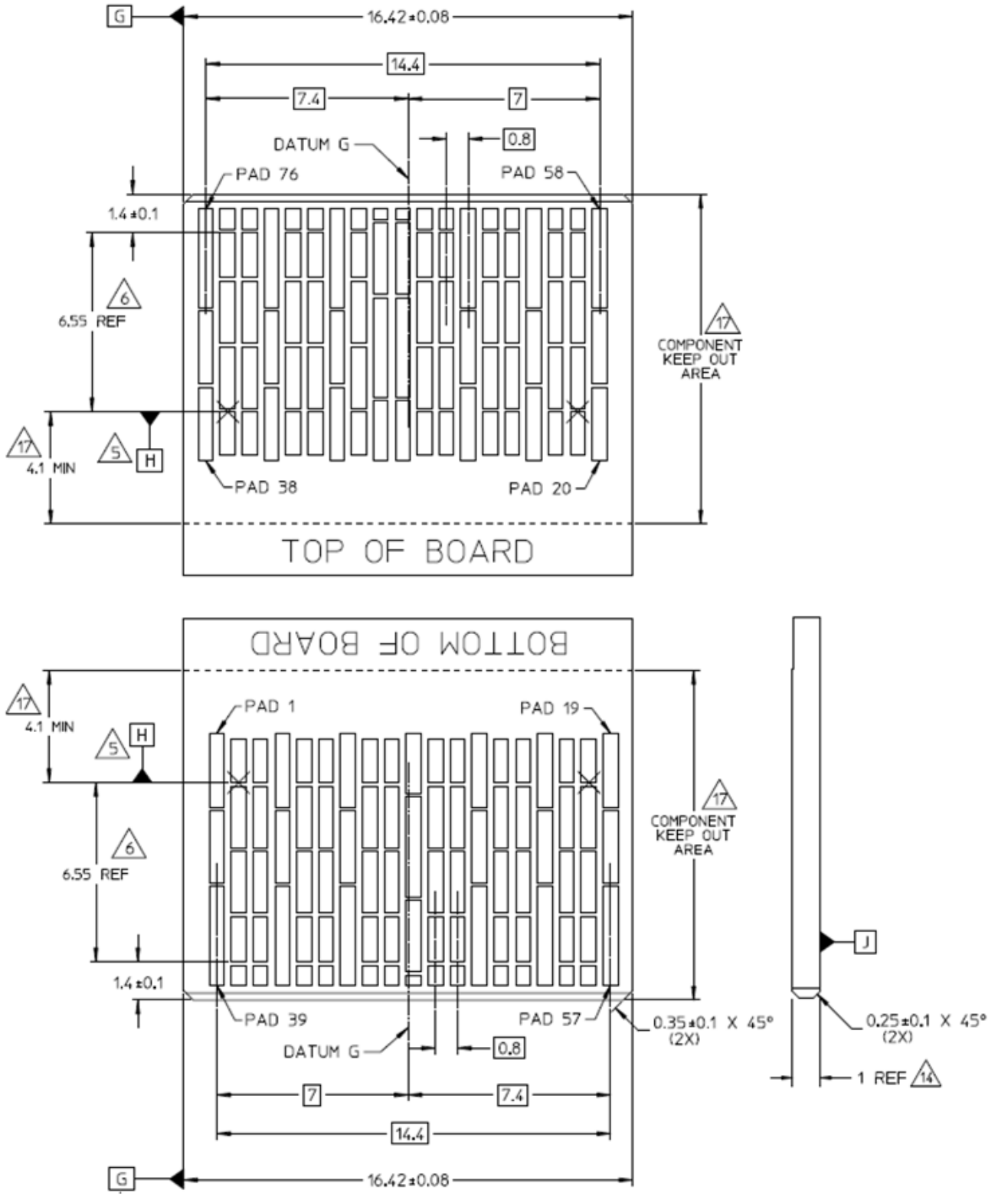


Figure 36: Module paddle card dimensions

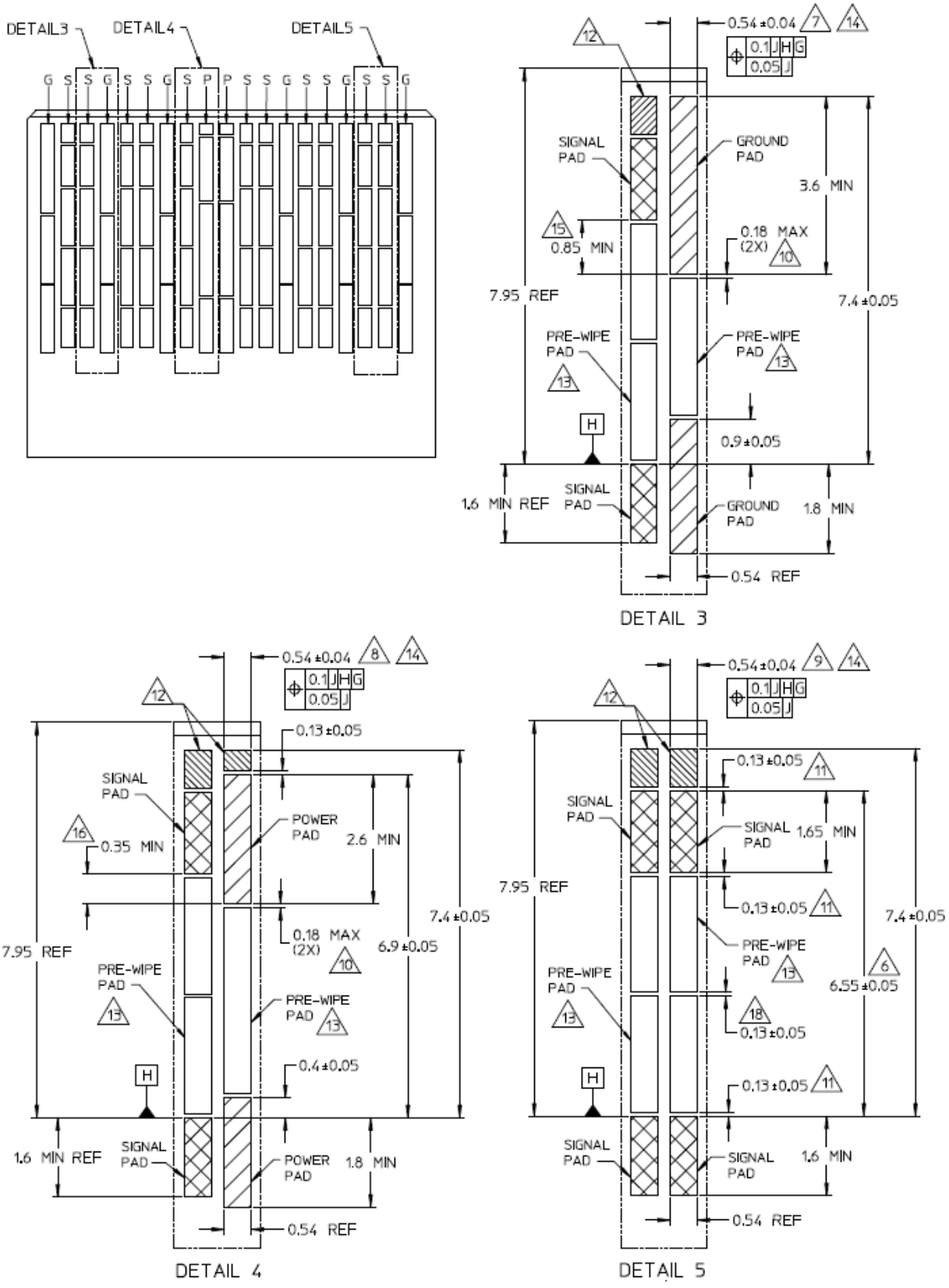


Figure 37: Module pad dimensions

6.6 Module Extraction and Retention Forces

The requirements for insertion forces, extraction forces and retention forces are specified in Appendix C. The contact pad plating shall meet the requirements in 6.5.

6.7 2x1 Electrical Connector Mechanical

The QSFP-DD Connector is a 76-contact, right angle connector. The integrated connector in a 2x1 stacked cage is shown in Figure 38 with detailed drawings in Figure 39, Figure 40 and Figure 41. Recommendations for the 2x1 stacked cage bezel opening are shown in Figure 42.

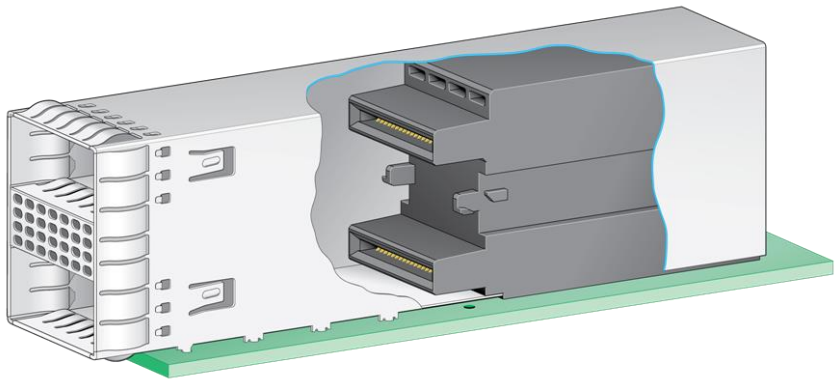


Figure 38: Integrated connector in 2x1 stacked cage

NOTES APPLY TO 2X1 STACKED CAGE :

1. DIMENSIONING AND TOLERANCING CONFORM TO ASME Y14.5-2009
2. ALL DIMENSIONS ARE IN MILLIMETERS.
3. DIMENSIONS FROM INSIDE SURFACES OF SPRING FINGERS WHEN FULLY DEPRESSED
4. CONNECTOR REMOVED FOR DRAWING CLARITY.
5. APPLIES TO ALL SPRING FINGERS ON ALL SIDES.
6. EXTERNAL CAGE DIMENSIONS. DOES NOT INCLUDE FOLDING TABS.
7. LENGTH OF CAGE AND SIGNAL TAILS.
8. PRESS FIT CAGE PINS APPLY TO RIGHT SIDE OF CAGE.
9. PRESS FIT CAGE PINS APPLY TO LEFT SIDE TO CAGE.
10. PRESS FIT PIN OFFSET BETWEEN RIGHT AND LEFT SIDE OF CAGE.
11. DIMENSIONS INCLUDES BACKCOVER.
12. SIZE AND POSITION OF CAGE AND CONNECTOR PRESS FIT PINS SHALL BE DEFINED BY EACH SUPPLIER BASED UPON THE PCB FOOTPRINT LAYOUT
13. CAVITY FOR HEAT SINK IS OPTIONAL
14. CONTACT PIN DIMENSION MEASURED FROM DATUM T
15. CONTACT PIN DIMENSION MEASURED FROM DATUM T1

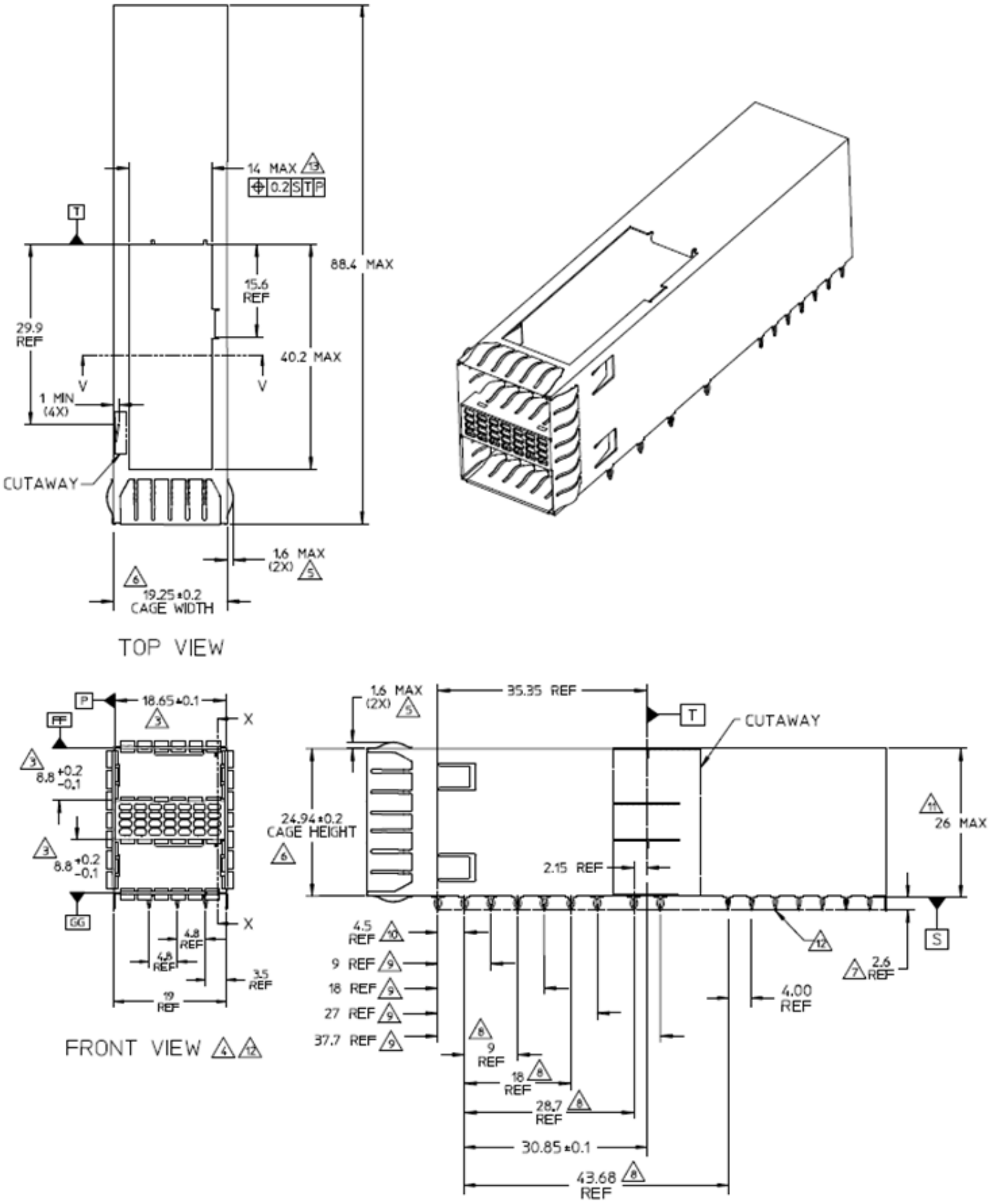


Figure 39: 2x1 stacked cage

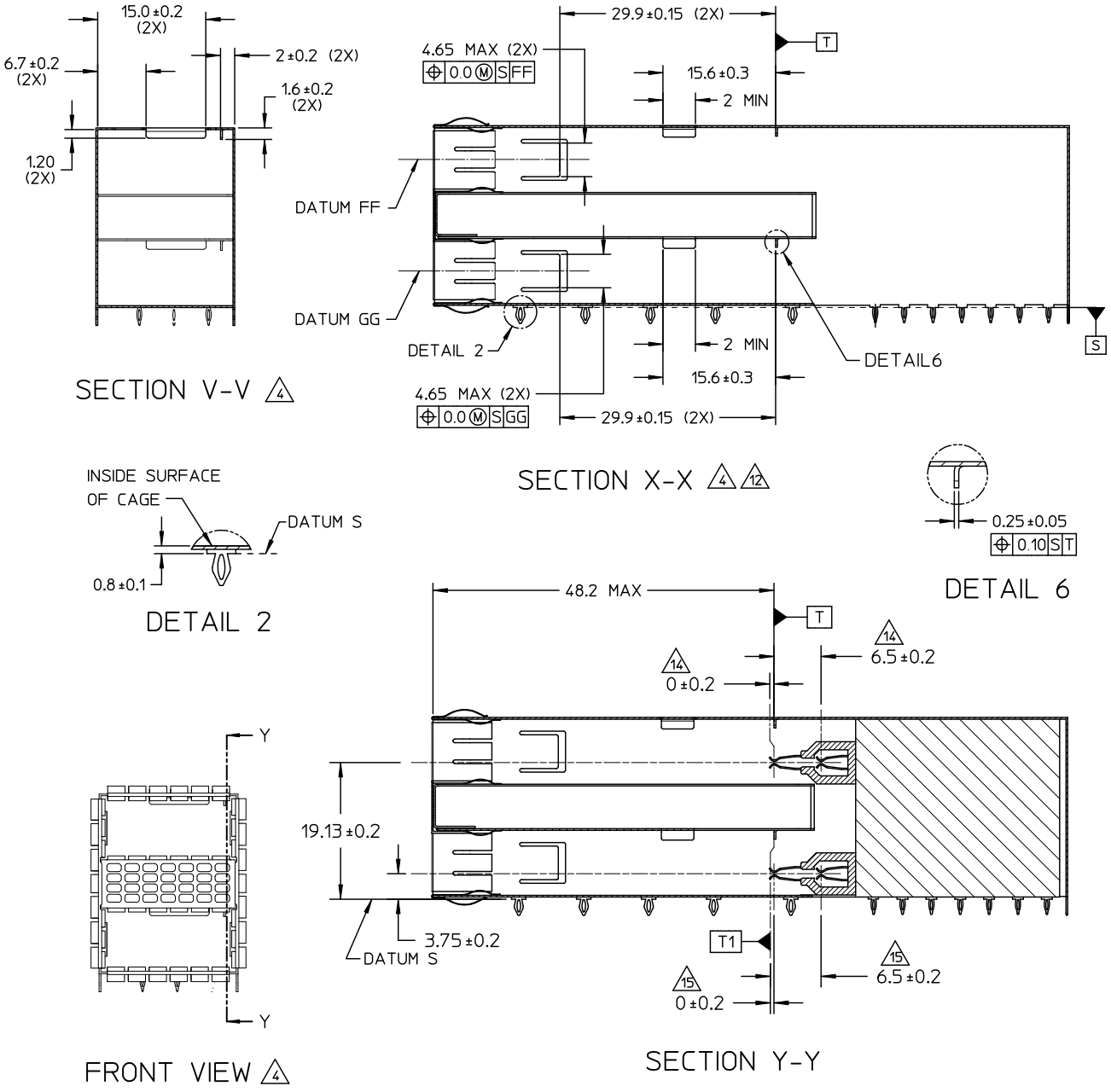


Figure 40: 2x1 stacked cage dimensions

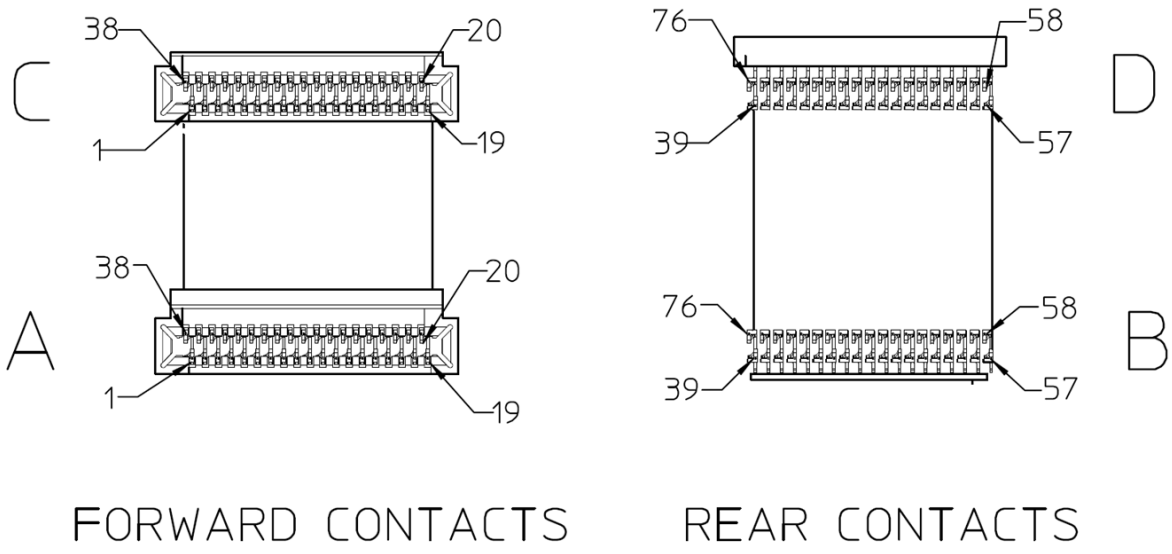


Figure 41: Connector pins in 2x1 stacked cage as viewed from front

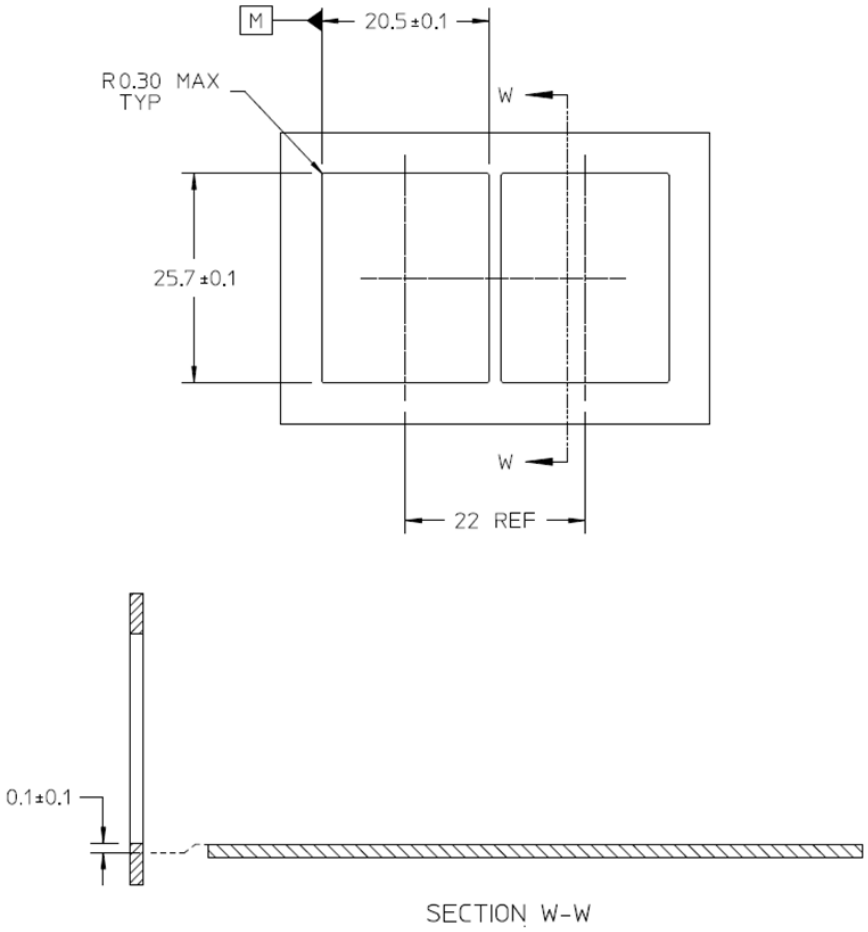


Figure 42: 2x1 Bezel Opening

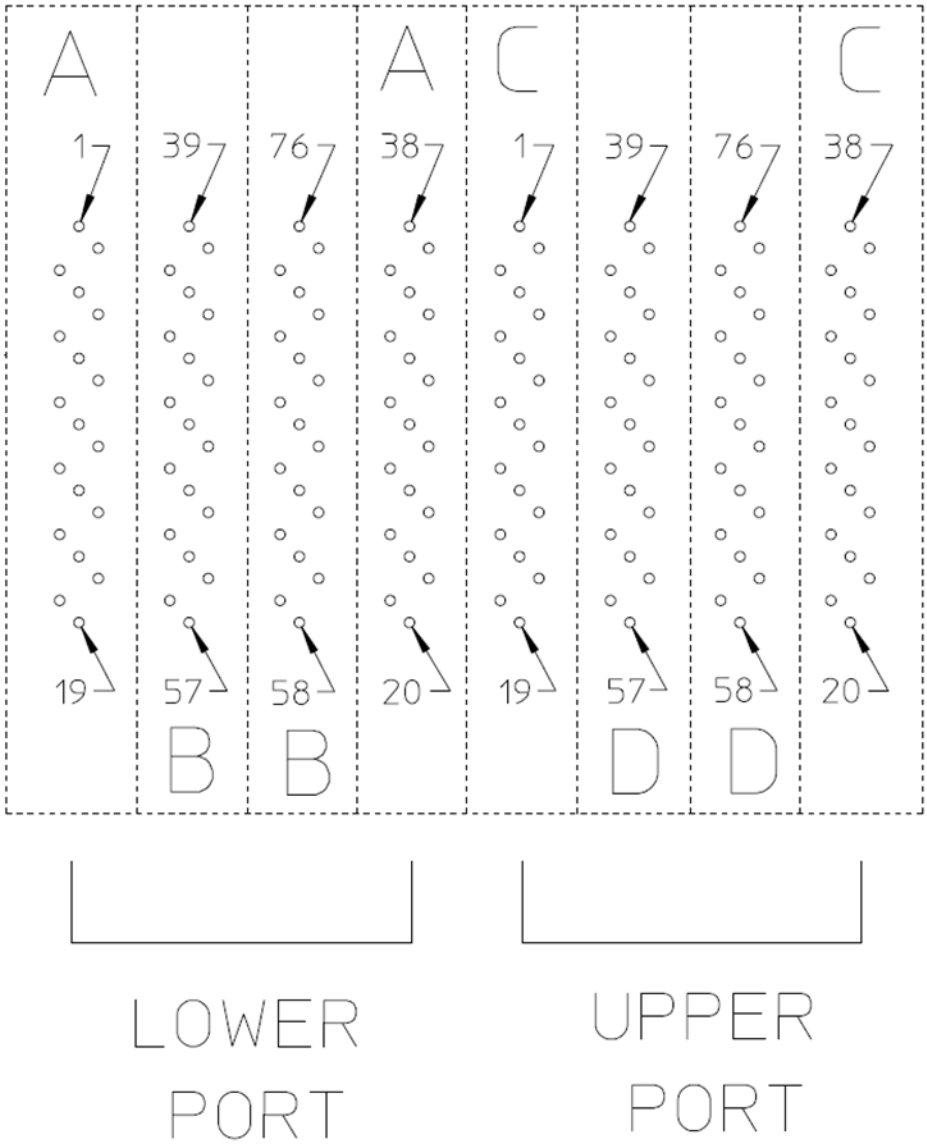


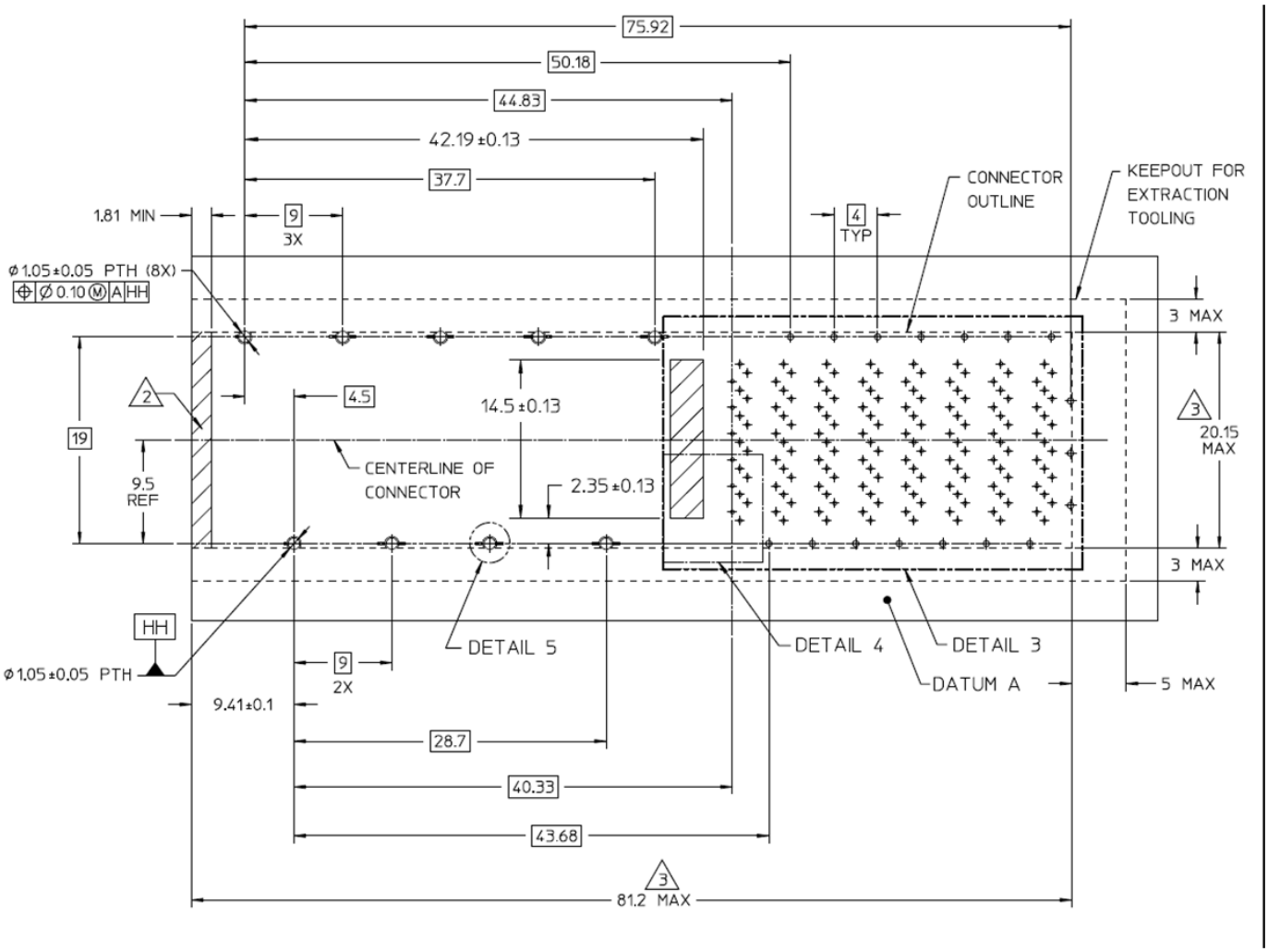
Figure 43: 2X1 host board connector contacts

6.7.1 2x1 Connector and Cage host PCB layout

A typical host board mechanical layout for attaching the QSFP-DD 2x1 Connector and Cage system is shown in Figure 43 and Figure 44. Location of the pattern on the host board is application specific. To achieve 25-50 Gbps performance pad dimensions and associated tolerance must be adhered to and attention paid to the host layout.

Notes for Host PCB (Figure 29):

1. The entire area under the connector (outside dashed lines) is to be considered a keep out area for components
2. Hatched area represent zones on the PCB that come in contact with or are in close proximity to the plastic housing or the connector cage. Indicated areas to be considered trace free.
3. Dimension applies to connector outline



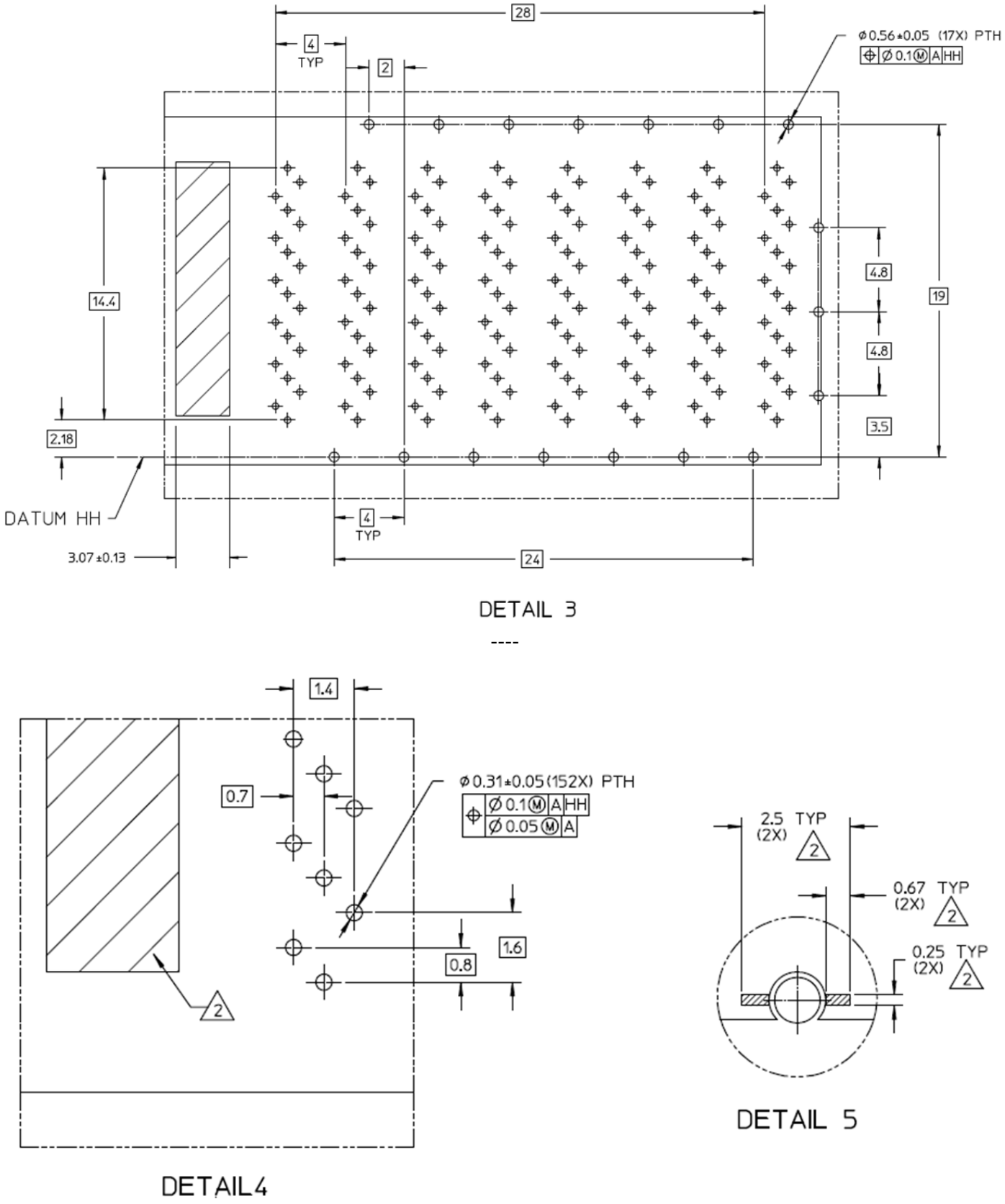


Figure 44: 2X1 Host PCB Mechanical Layout

6.8 Surface Mount Electrical Connector Mechanical

The QSFP-DD Connector is a 76-contact, right angle connector. The SMT connector in a 1xn cage is shown in Figure 45 with detailed drawings in Figure 46 and Figure 47 Recommendations for the SMT cage bezel opening are shown in Figure 48.

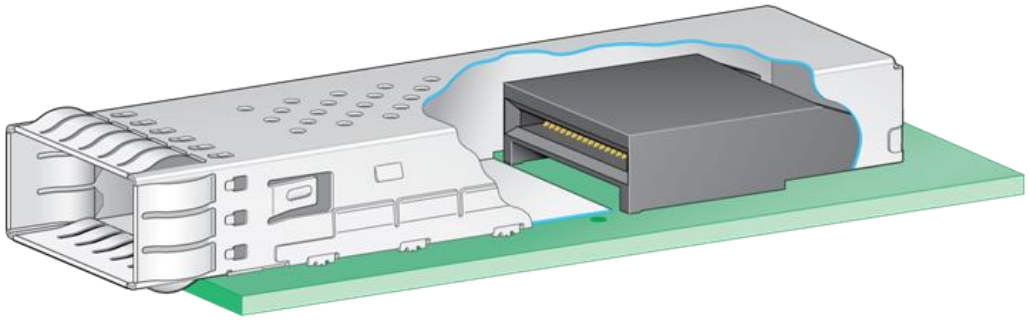


Figure 45: SMT connector in 1xn cage

Notes apply to SMT 1xN cage drawing, see Figure 45, Figure 46 and Figure 47.

1. DIMENSIONING AND TOLERANCING CONFORM TO ASME Y14.5-2009

2. ALL DIMENSIONS ARE IN MILLIMETERS.

3 DIMENSIONS FROM INSIDE SURFACES OF SPRING FINGERS WHEN FULLY DEPRESSED

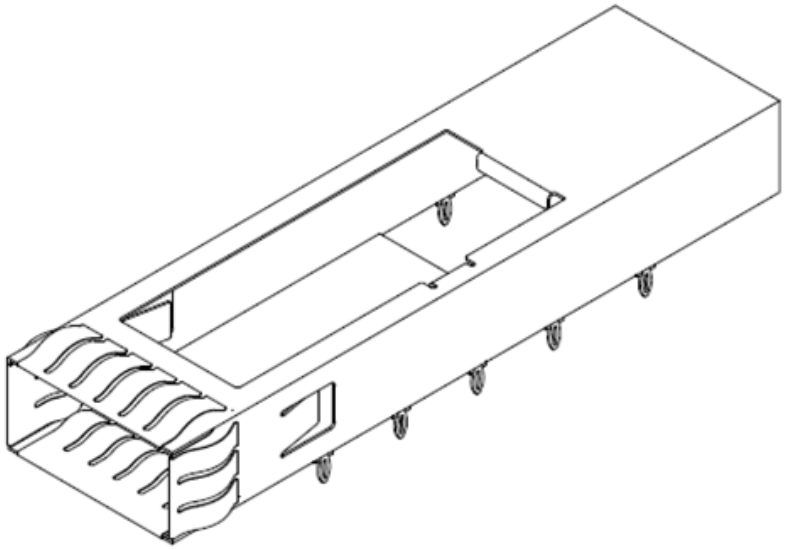
4 CAVITY FOR HEATSINK IS OPTIONAL

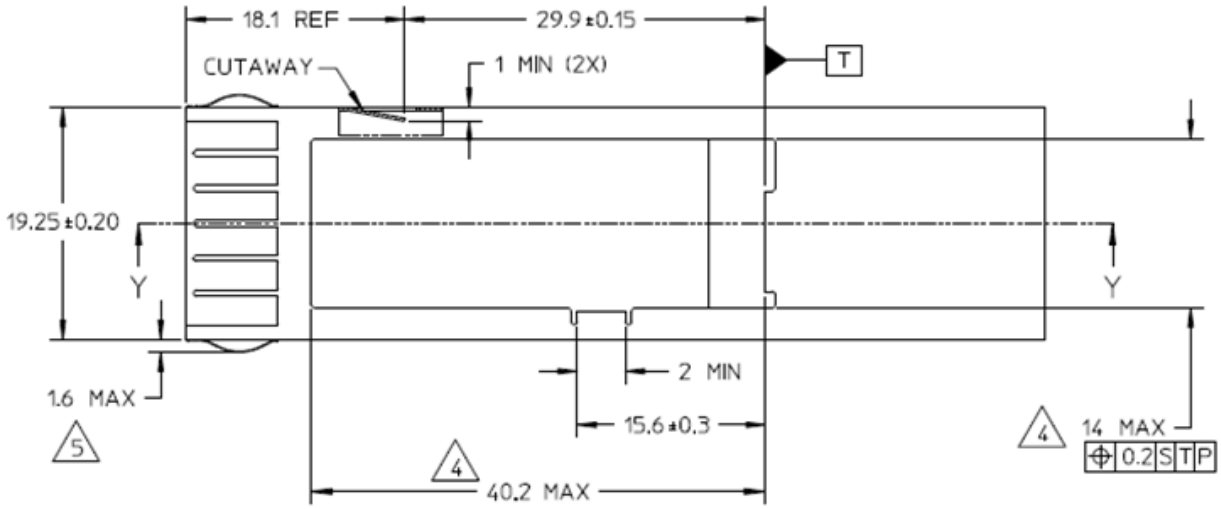
5 APPLIES TO ALL SPRING FINGERS ON ALL SIDES.

6 DATUM S IS DEFINED BY SEATING PLANE ON HOST BOARD

7 SIZE OF CAGE PRESS FIT PINS SHALL BE DEFINED BY EACH SUPPLIER BASED UPON THE PCB FOOTPRINT LAYOUT

8 THIS SURFACE REFERENCES POTENTIAL FEATURES TO SUPPORT MODULES




18.1 REF
29.9±0.15
CUTAWAY
1 MIN (2X)
T
19.25±0.20
Y
Y
1.6 MAX
5
2 MIN
15.6±0.3
4
40.2 MAX
4
14 MAX
0.2 S T P

TOP VIEW

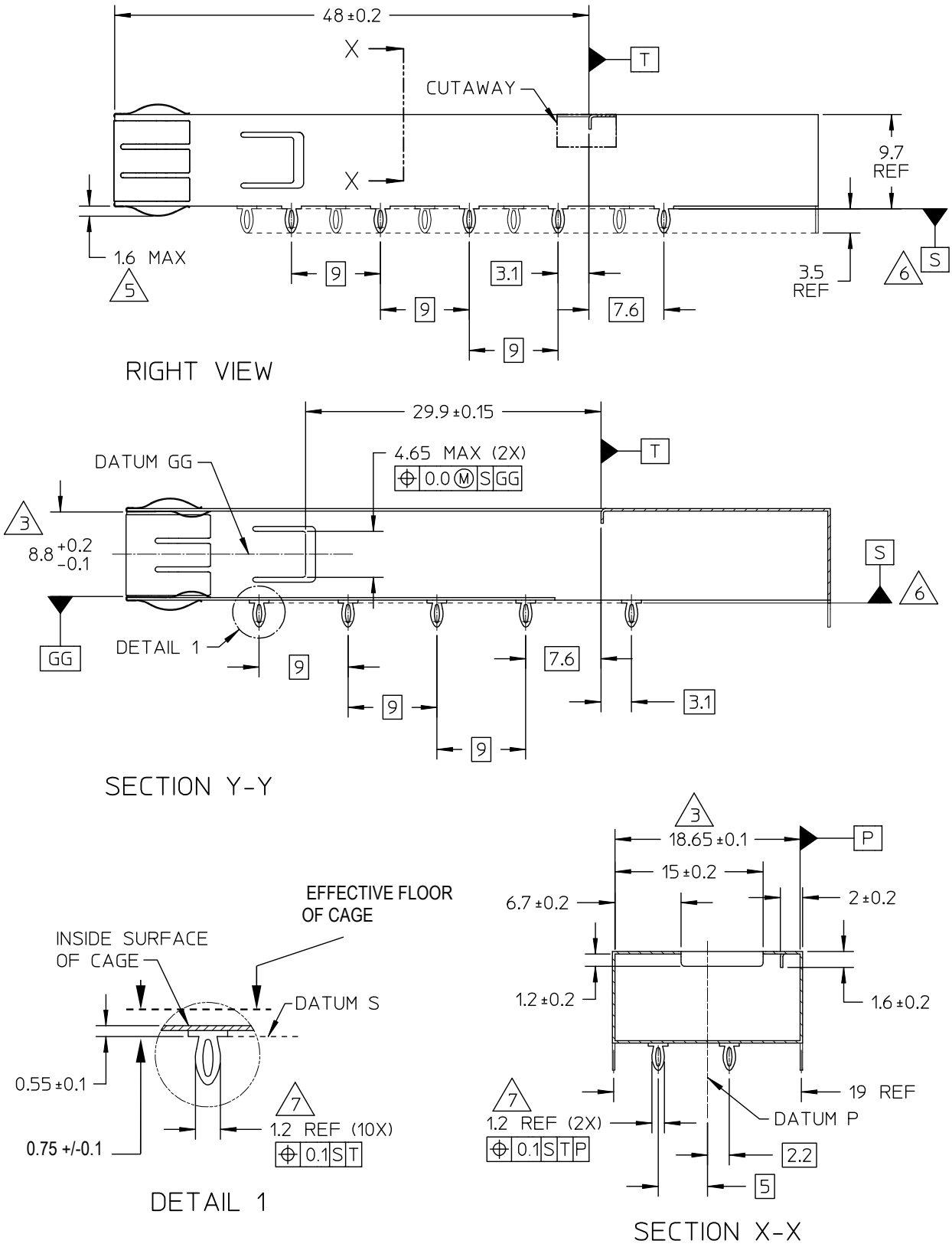
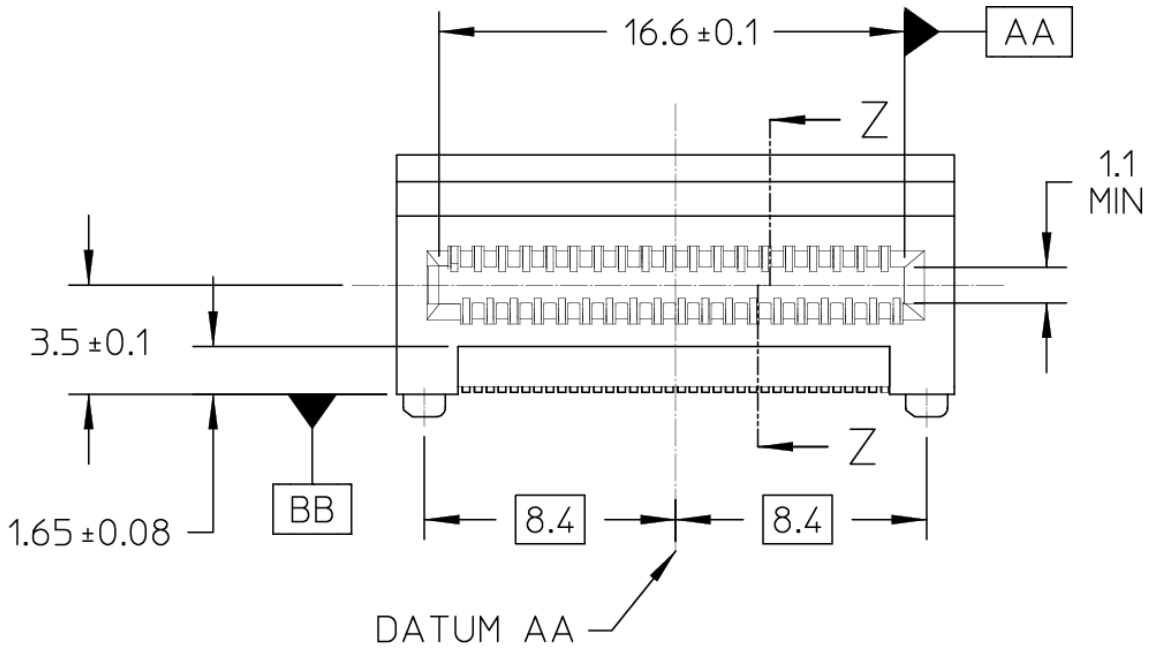
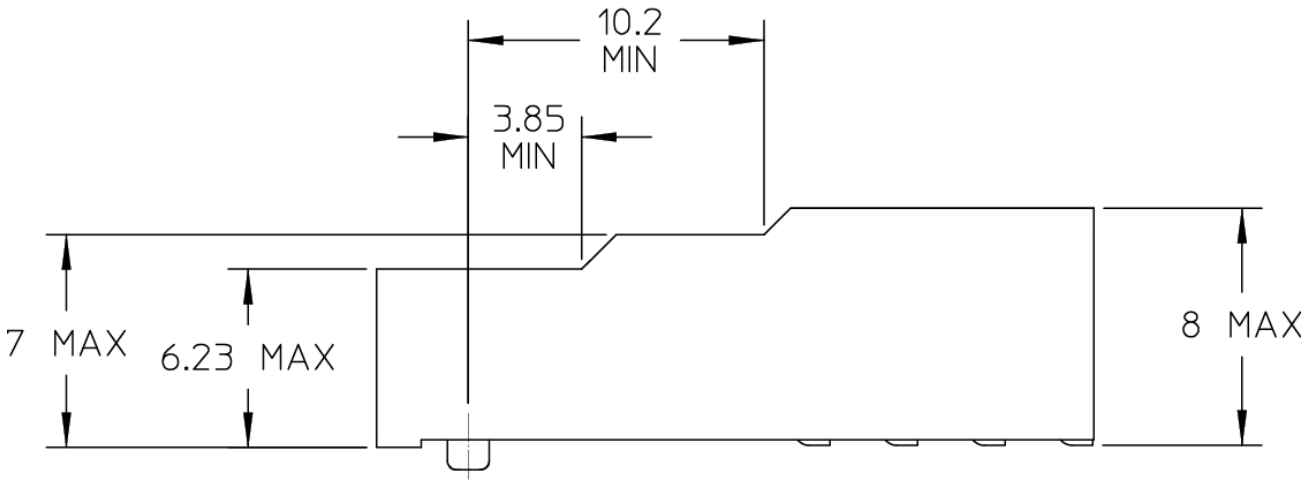


Figure 46: SMT 1x1 Cage Design



FRONT VIEW



SIDE VIEW

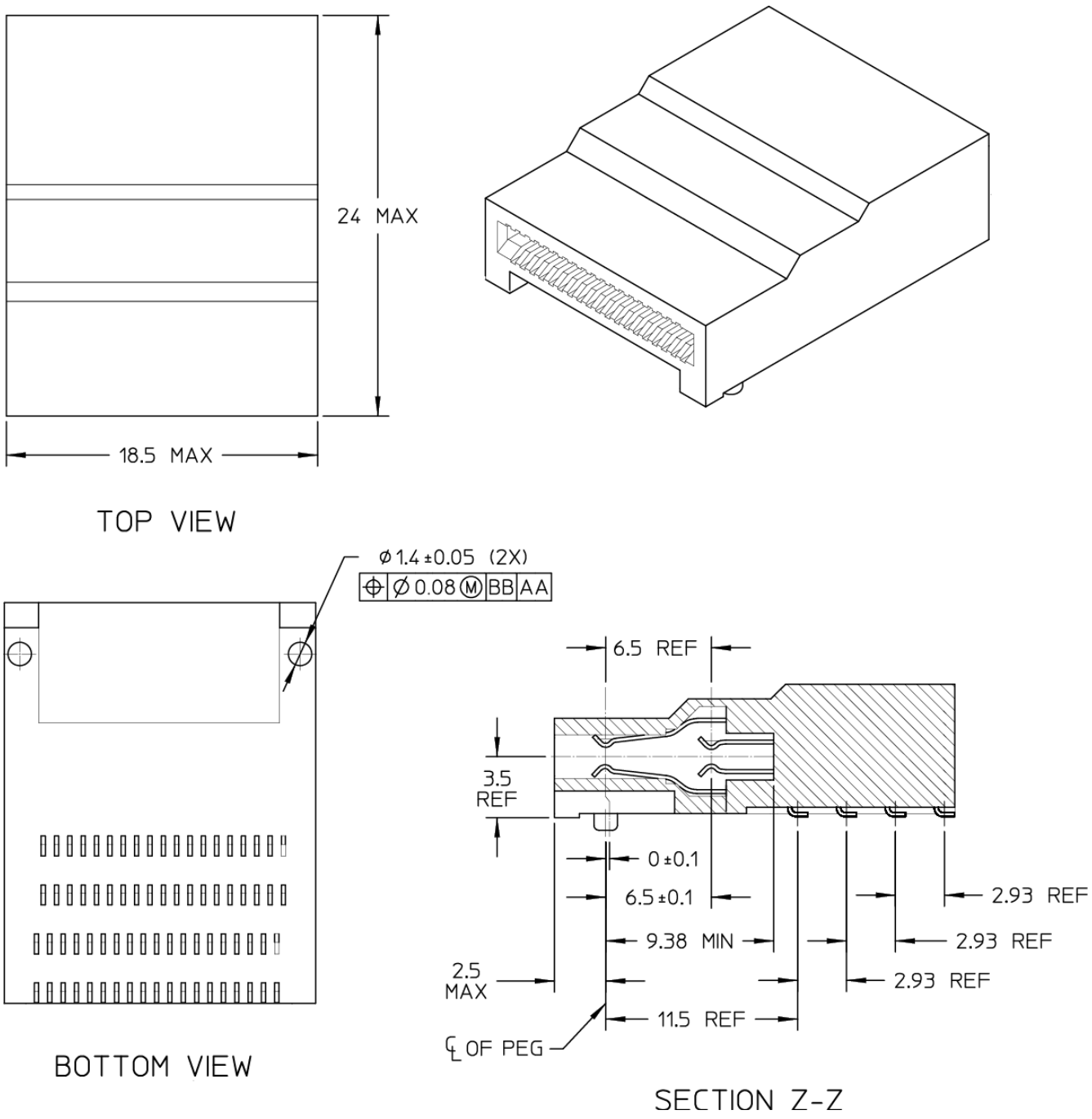


Figure 47: SMT 1x1 Connector Design

Note: Contact Pin Dimension Measured from Datum T

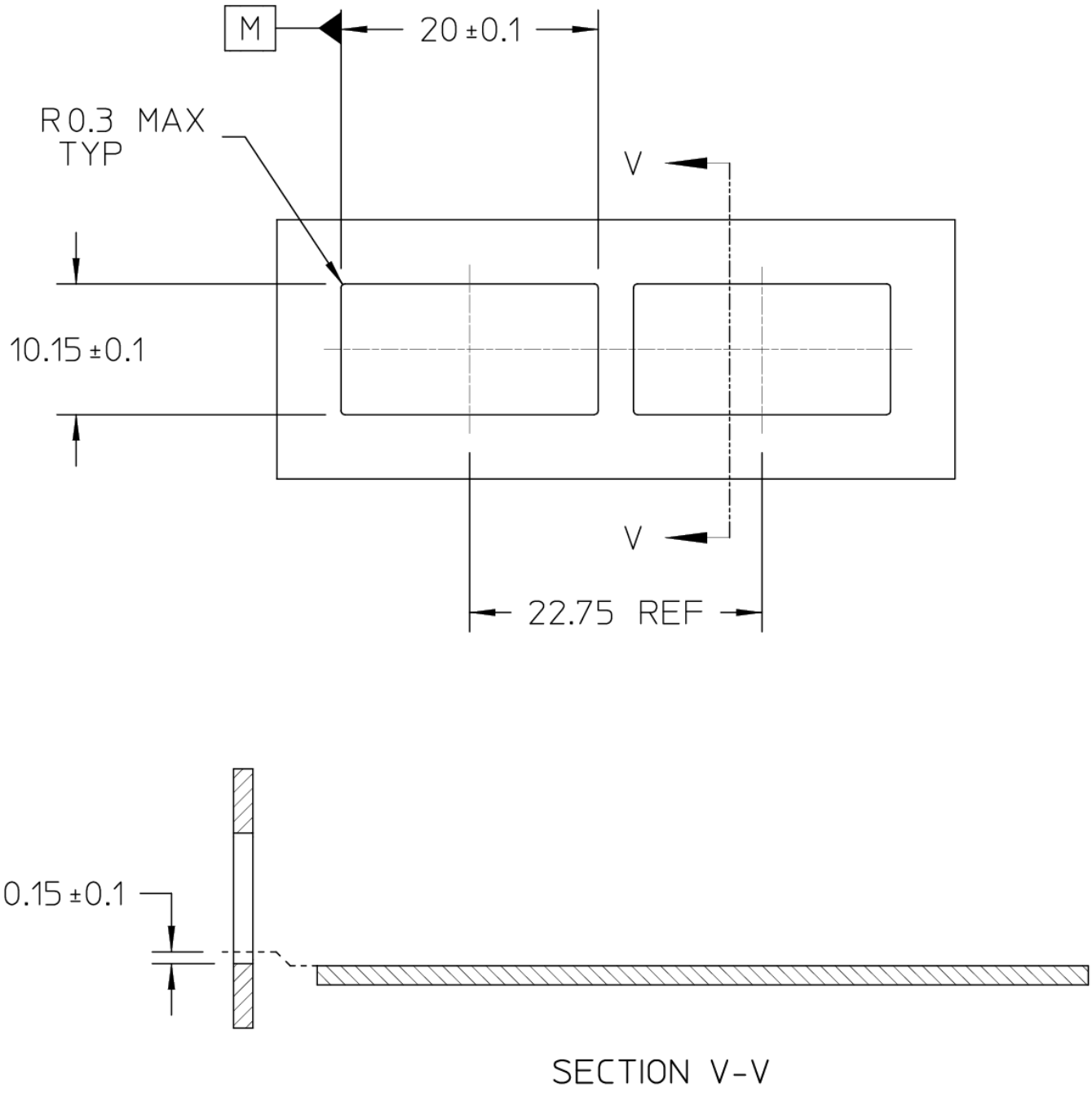


Figure 48: SMT 1x1 bezel opening

6.8.1 Surface mount connector and cage host PCB layout

A typical host board mechanical layout for attaching the QSFP-DD surface mount Connector and Cage System is shown in Figure 49 and Figure 50. Location of the pattern on the host board is application specific.

To achieve 25-50 Gbps performance pad dimensions and associated tolerances must be adhered to and attention paid to the host board layout.

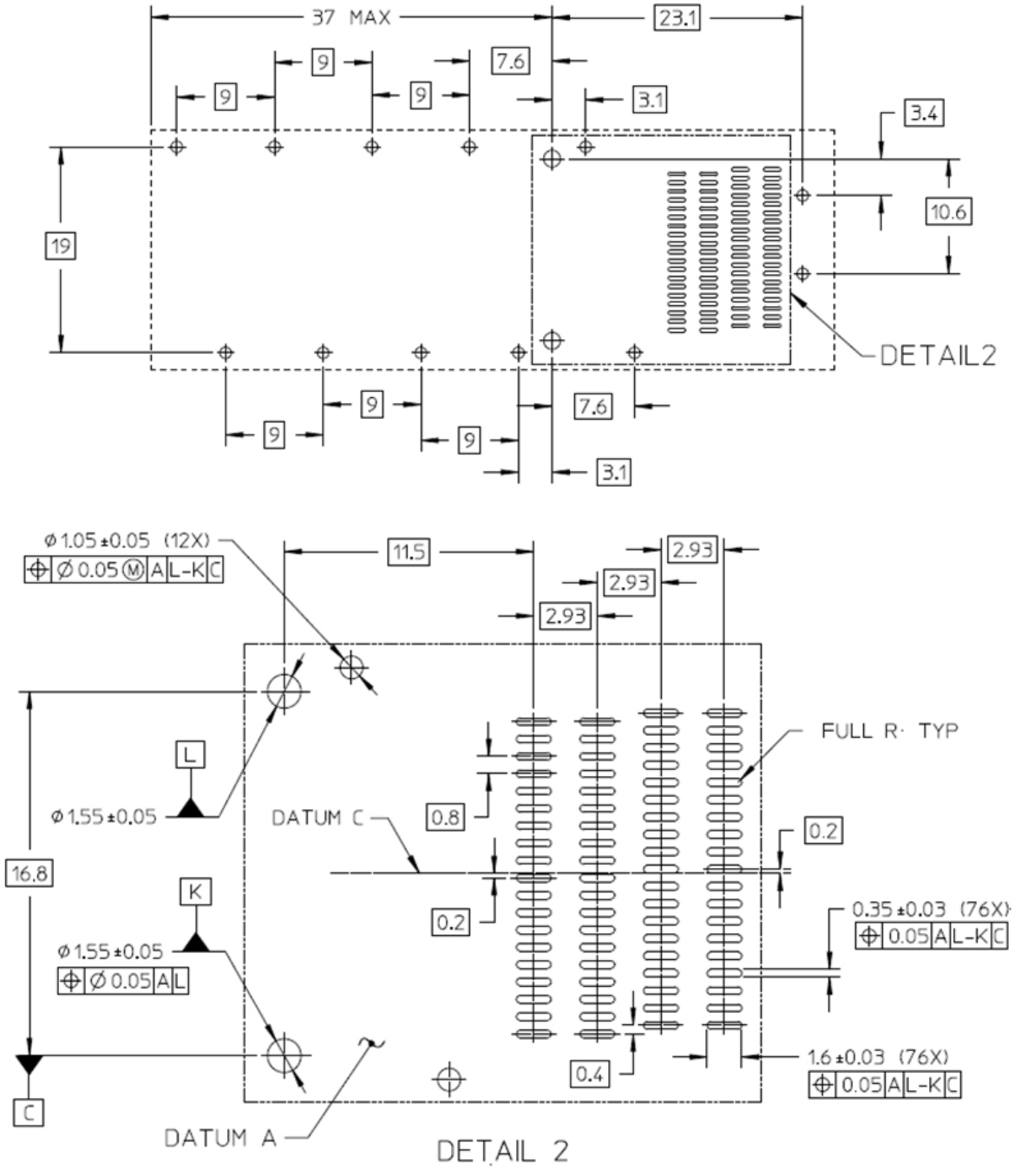


Figure 49: SMT Host PCB Mechanical Layout

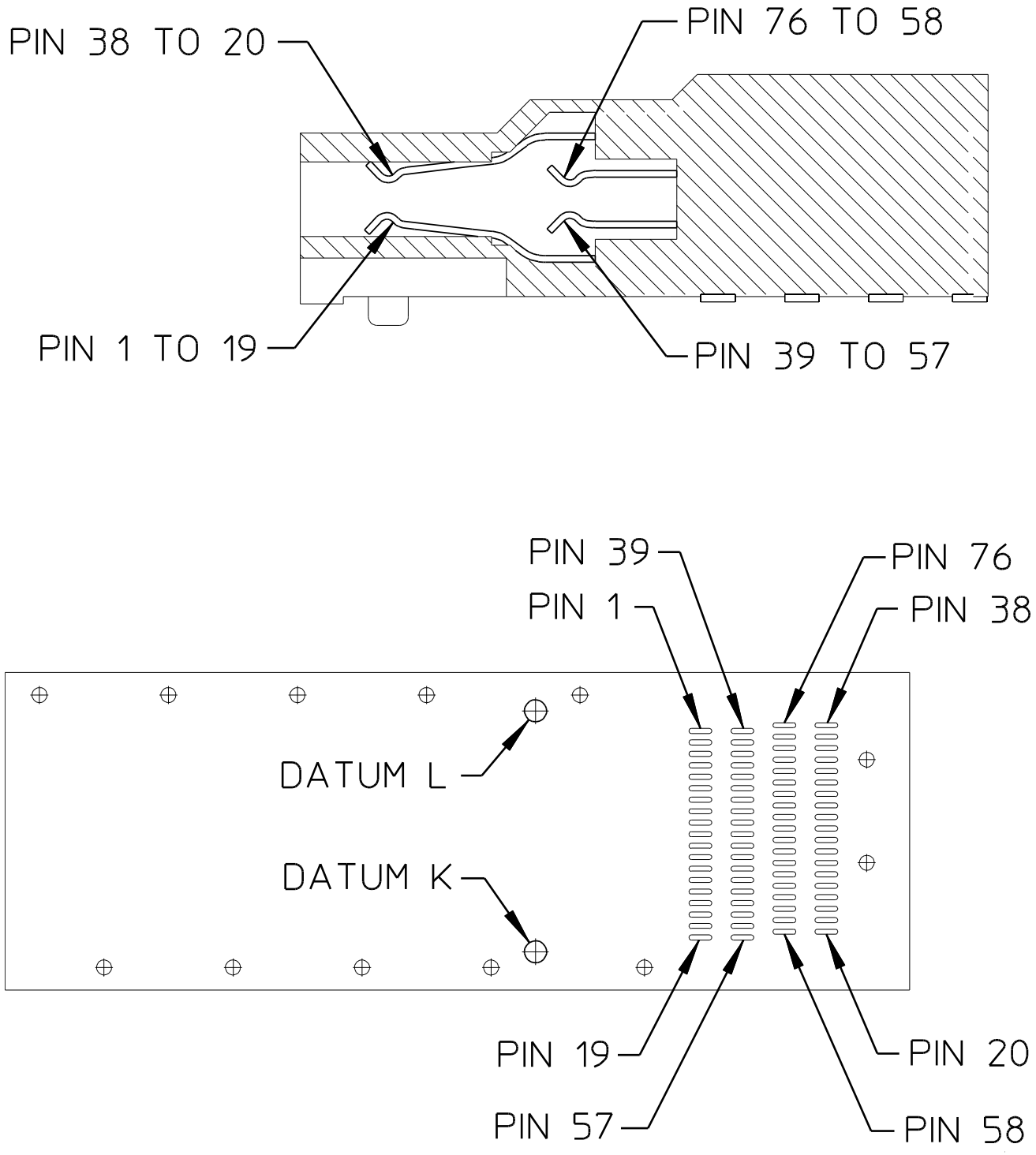


Figure 50: SMT Connector and Host PCB Pin Numbers

7 QSFP-D Module Environmental and Thermal Requirements

QSFP-DD is designed to allow for up to 36 modules; stacked, ganged and/or belly-to-belly in a 1U 19" rack, with the appropriate thermal design for cooling/airflow.

The equipment supplier is responsible for controlling the module case temperature to the specified range. The module supplier is responsible for defining a point on the module case where the temperature is measured. This should be a point connected to an internal component with the least thermal margin, e.g. a laser diode. It is recommended that the defined point on the module case be behind the equipment faceplate in order to enable in-system monitoring.

7.1 Thermal Requirements

The module case temperature may be within one or more of the case temperatures ranges defined in Table 12. The temperature ranges are applicable between 60 m below sea level and 1800m above sea level, utilizing the host systems designed airflow. For further information see Telcordia GR-63-CORE, Issue 5, December 2017, NEBSTM Requirements: Physical Protection.

Table 12- Temperature Range Class of operation

Class	Module Case Temperature
Standard	0°C through 70°C
Extended	-5°C through 85°C
Industrial	-40°C through 85°C

7.2 Thermal Requirements – tighter controlled environments

The classes in Table 13 are intended for tighter controlled environments, e.g. data center environments as described in *"Thermal guidelines for data processing environments", fourth Ed., ASHRAE, 2015.* The four classes correspond to different ranges of equipment intake air temperature.

Table 13- Temperature Range Classes for Tighter Controlled Applications

Class	Module Functional Case Temperature[1]	Module Case Temperature[2]
A1	15°C to 62°C	25°C to 62°C
A2	10°C to 65°C	20°C to 65°C
A3	5°C to 70°C	15°C to 70°C
A4	5°C to 75°C	15°C to 75°C

Notes:
1. Functional includes all features available in Low Power Mode.
2. Module case temperature means all specifications are met in high power mode.

7.3 External Case and Handle Touch Temperature

For all power classes, all module case and handle surfaces outside of the cage must comply with applicable touch temperature requirements. If the module case temperature will exceed applicable short-term touch temperature limits, a means must be provided to prevent contact with the case during unlatching and removal. Figure 26, Figure 27 and Appendix A show typical handles used to unlatch and remove the module, thereby limiting contact with the module case. Handles are typically low thermal conductivity elastomer and allow for a higher touch temperature. For more information see "*IEC/UL 60950-1* Requirements for Information Technology Equipment" and "*Telcordia GR-63-CORE, Issue 5, December 2017, NEBS™ Requirements: Physical Protection".*

Appendix A Informative overall module length with elastomeric handle

Figure 51 and Figure 52 show flexible elastomeric handles attached to the module latches. Handle ends for Types 1 and Type 2 modules should be aligned independent of module case extension. Type 1 modules should meet the overall length of 118 mm maximum per Figure 51 with a handle length of approximately 50mm. Type 2 modules should comply with Figure 52 and have reduced handle length equal to the module case length extension.

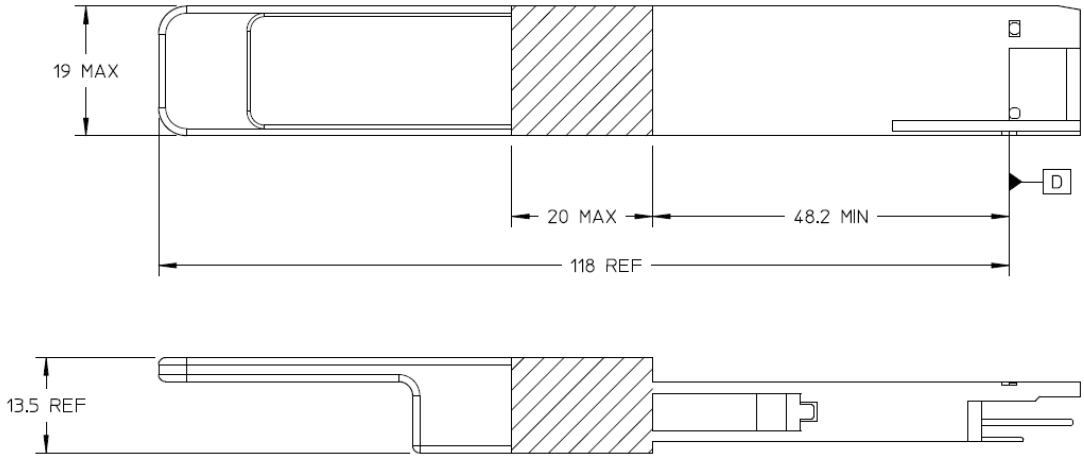


Figure 51: Informative overall module length with handle for Type 1 module

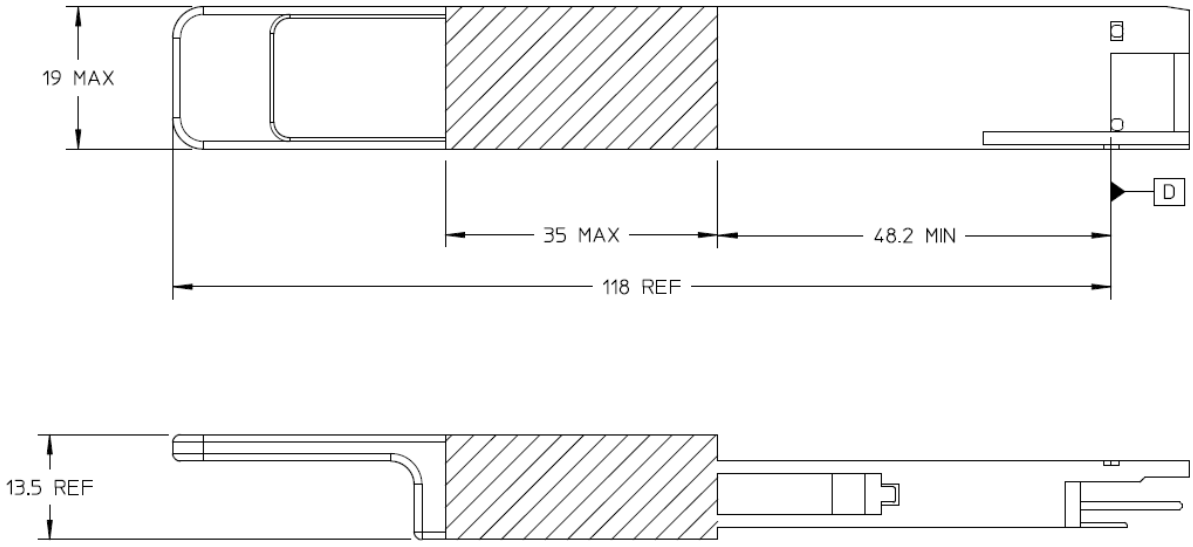


Figure 52: Informative overall module length with handle for Type 2 and Type 2A modules

Appendix B Informative Module Type 2A Heat Sink Examples

This appendix contains several designs examples of higher power Type 2A modules with heat sinks.

Thermal design is system dependent; however, systems seeking to maximize the benefit of the external heat sink of Type 2A modules should consider minimizing bypass of airflow through the external heat sink. One potential method is to use a minimal gap between the outer surface of the front panel and the trailing edge of the external heat sink fins as shown in this appendix. Type 2A example module insertion is shown in Figure 53. Type 2A example of 1X1 bezel design is shown in Figure 54. Type 2A example of 2X1 bezel design is shown in Figure 55. Type 2A extruded heat sink example is shown in Figure 56. Type 2A die cast heat sink with metal cover example is shown in Figure 57. Type 2A Zipper fin heat sink example is shown in Figure 58.

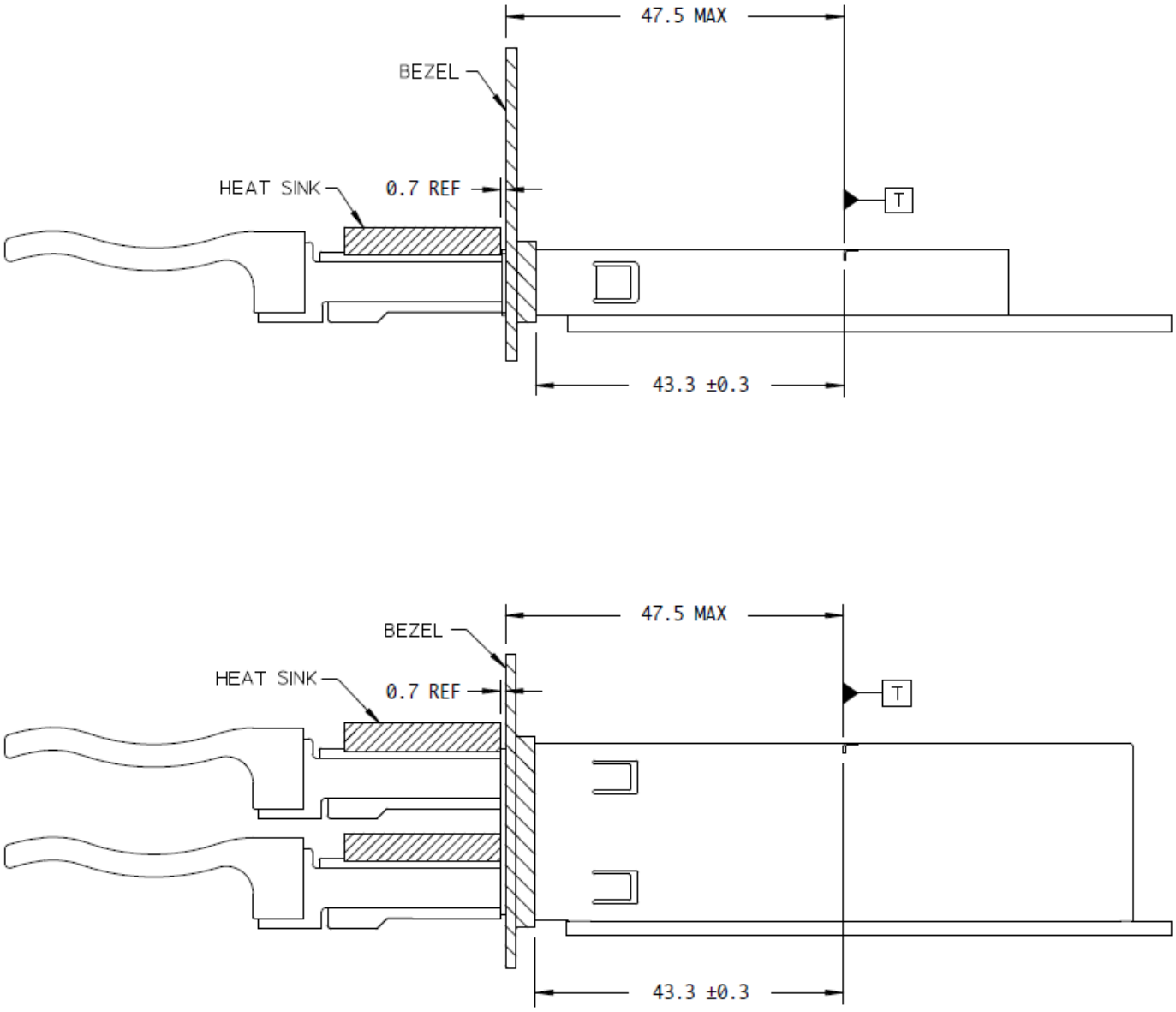


Figure 53: Type 2A example module insertion

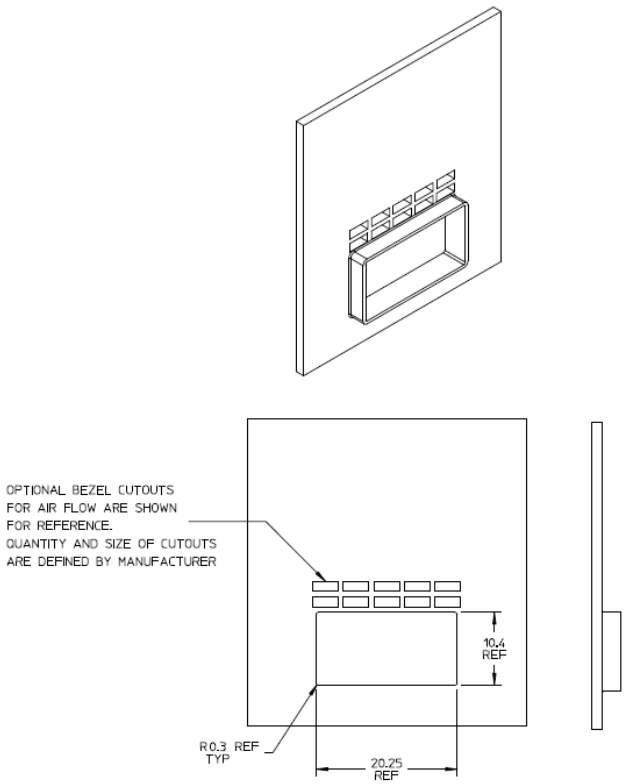


Figure 54: Type 2A example 1X1 bezel design

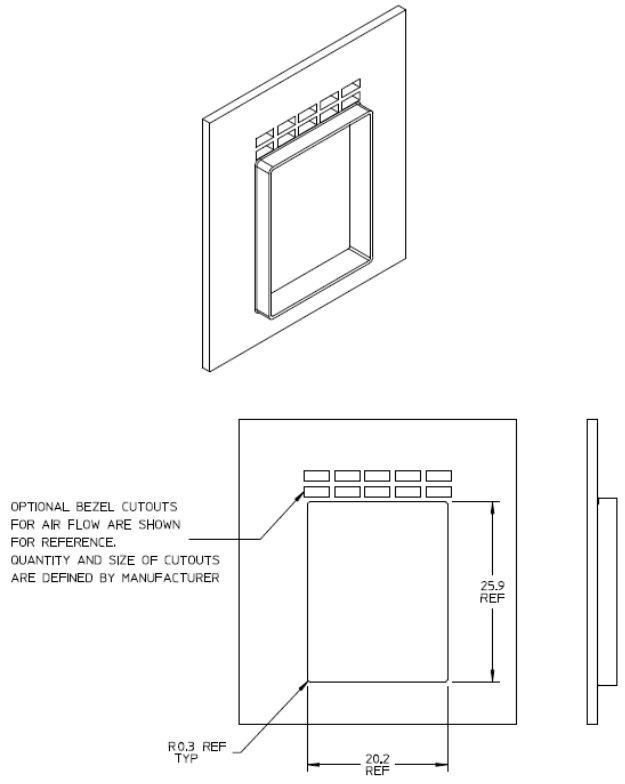


Figure 55: Type 2A example 2X1 bezel design

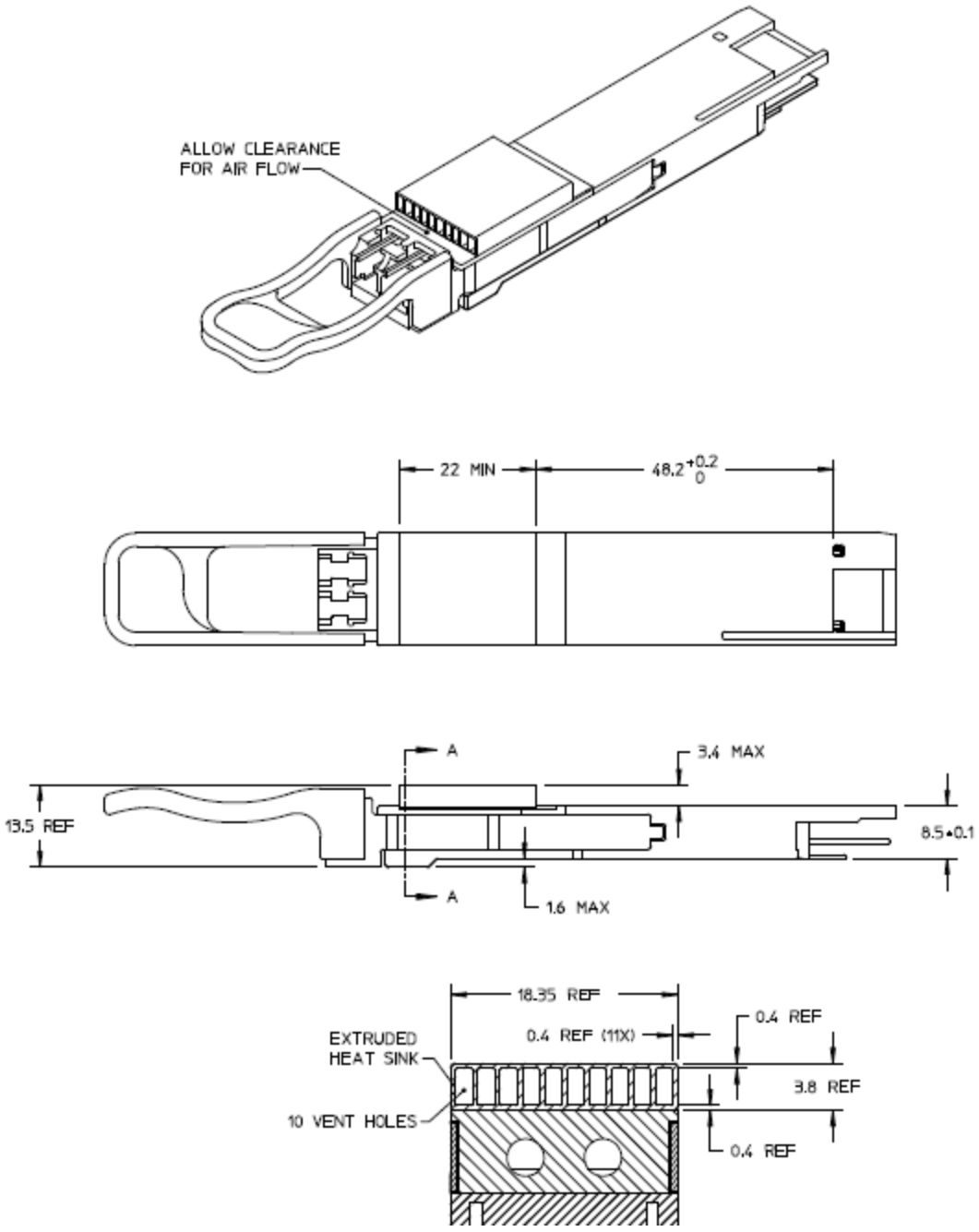


Figure 56: Type 2A Extruded Heat Sink Example

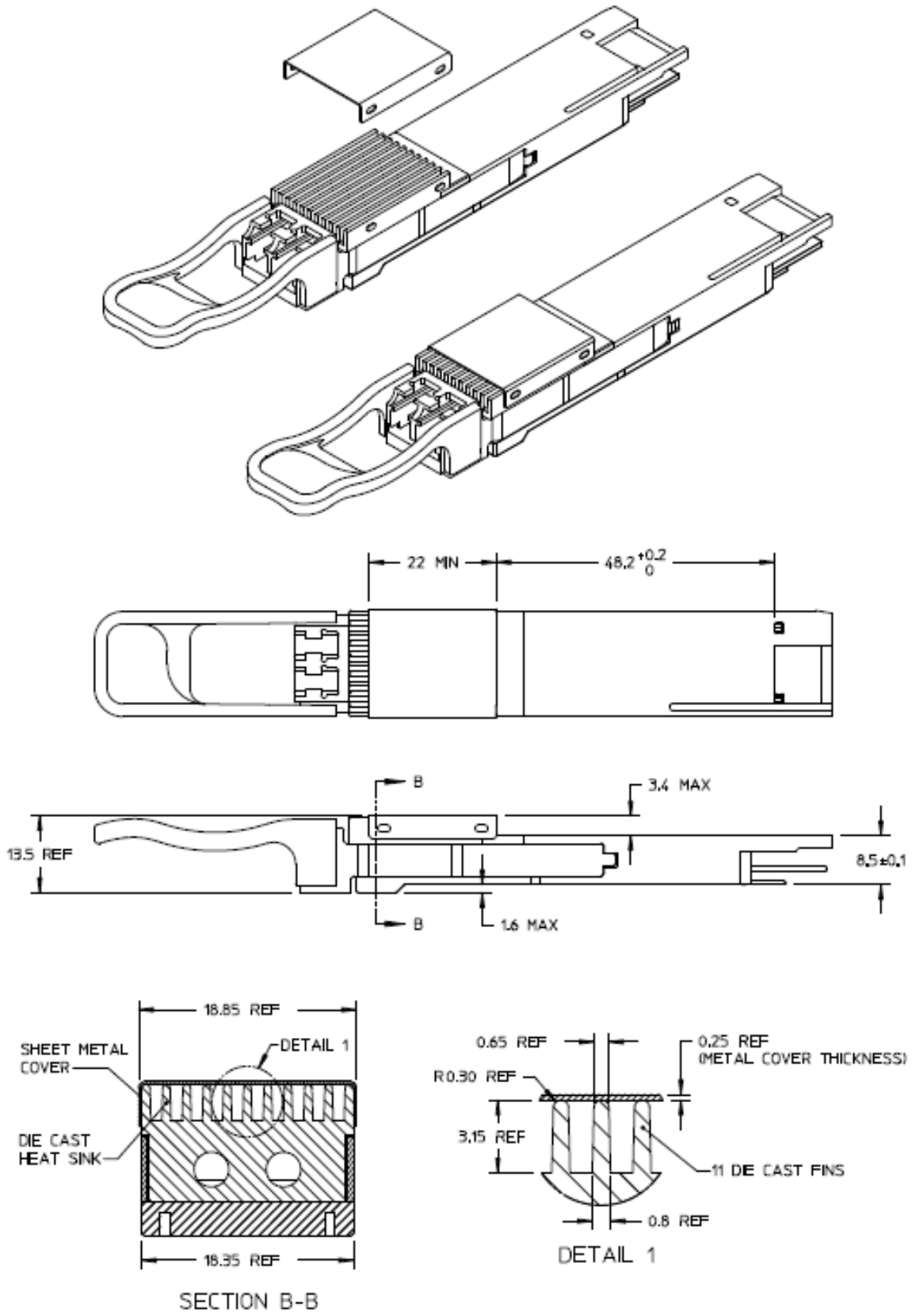


Figure 57: Type 2A Die Cast Heat Sink with Metal Cover Example

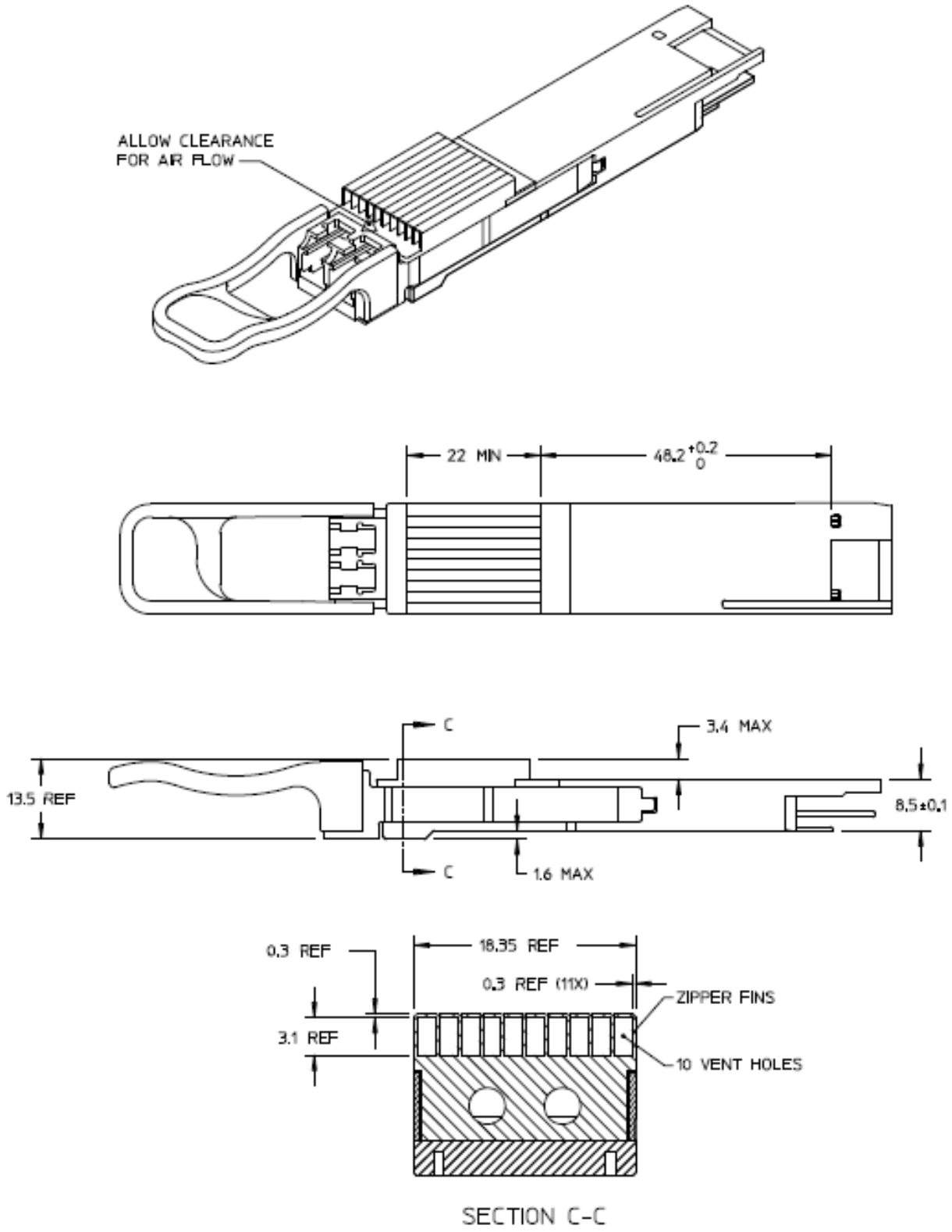


Figure 58: Type 2A Zipper Fin Heat Sink Example

Appendix C Normative Module and Connector Performance Requirements

C.1 Performance Tables

EIA-364-1000 (TS-1000) shall be used to define the test sequences and procedures for evaluating the connector system described in this document. Where multiple test options are available, the manufacturer shall select the appropriate option where not previously specified. The selected procedure should be noted when reporting data. If there are conflicting requirements or test procedures between EIA-364 procedures and those contained within this document, this document shall be considered the prevailing authority. Unless otherwise specified, procedures for sample size, data, and collection to be followed as specified in EIA-364-1000. See EIA-364-1000 Annex B for objectives of tests and test groups.

This document represents the minimum requirements for the defined product. Additional test conditions and evaluations may be conducted within the defined EIA-364-1000 sequences. More extreme test conditions and failure criteria may be imposed and still meet the requirements of this document.

Table 14 summarizes the performance criteria that are to be satisfied by the connector described in this document. Most performance criteria are validated by EIA-364-1000 testing, but this test suite leaves some test details to be determined. To ensure that testing is repeatable, these details are identified in Table 15. Finally, testing procedures used to validate any performance criteria not included in EIA-364-1000 are provided in Table 16.

Table 14- Form Factor Performance Requirements

Performance Parameters	Description/ Details	Requirements
Mechanical/ Physical Tests		
Plating Type	Plating type on connector contacts	Precious (refer to 6.5 for plating details)
Surface Treatment	Surface treatment on connector contacts; if surface treatment is applied, Test Group 6 is required	Manufacturer to specify
Wipe length	Designed distance a contact traverses over a mating contact surface during mating and resting at a final position. If less than 0.127 mm, test group 6 is required	Manufacturer to specify
Rated Durability Cycles	The expected number of durability cycles a component is expected to encounter over the course of its life	Connector/ cage: 100 cycles Module: 50 cycles
Mating Force[1]	Amount of force needed to mate a module with a connector when latches are deactivated	QSFP module: 40 N MAX QSFP-DD module: 90 N MAX
Unmating Force[1]	Amount of forced needed to separate a module from a connector when latches are deactivated	QSFP module: 30 N MAX QSFP-DD module: 50 N MAX
Latch Retention[1]	Amount of force the latching mechanism can withstand without unmating	QSFP module: 90 N MIN QSFP-DD module: 90 N MIN
Cage Latch Strength[1]	The amount of force that the cage latches can hold without being damaged.	125 N MIN
Cage Retention to Host Board[1]	Amount of force a cage can withstand without separating from the host board	114 N MIN
Environmental Requirements		
Field Life	The expected service life for a component	10 years
Field Temperature	The expected service temperature for a component	65°C
Electrical Requirements		
Current	Maximum current to which a contact is exposed in use	0.5 A per signal contact MAX 1.0 A per power contact MAX
Operating Rating Voltage	Maximum voltage to which a contact is exposed in use	30 V DC per contact MAX

Note:
1. These performance criteria are not validated by EIA-364-1000 testing, see Table 16 for test procedures and pass/fail criteria.

Table 15 describes the details necessary to perform the tests described in the EIA-364-1000 test sequences. Testing shall be done in accordance with EIA-364-1000 and the test procedures it identifies in such a way that the parameters/ requirements defined in Table 14 are met. Any information in this table supersedes EIA-364-1000.

Table 15- EIA-364-1000 Test Details

Performance Parameters	Description/ Details	Requirements
Mechanical/ Physical Tests		
Durability (preconditioning)	EIA-364-09 To be tested with connector, cage, and module. Latches may be locked out to aid in automated cycling.	No evidence of physical damage
Durability[1]	EIA-364-09 To be tested with connector, cage, and module. Latches may be locked out to aid in automated cycling.	No visual damage to mating interface or latching mechanism
Environmental Tests		
Cyclic Temperature and Humidity	EIA-364-31 Method IV omitting step 7a Test Duration B	No intermediate test criteria
Vibration	EIA-364-28 Test Condition V Test Condition Letter D Test set-up: Connectors may be restrained by a plate that replicates the system panel opening as defined in this specification. External cables may be constrained to a non-vibrating fixture a minimum of 8 inches from the module. For cabled connector solutions: Wires may be attached to PCB or fixed to a non-vibrating fixture.	No evidence of physical damage -AND- No discontinuities longer than 1 µs allowed
Mixed Flowing Gas	EIA-364-65 Class II See Table 4.1 in EIA-364-1000 for exposure times Test option Per EIA-364-1000 option 3	No intermediate test criteria
Electrical Tests		
Low Level Contact Resistance[2]	EIA-364-23 20 mV DC Max, 100 mA Max To include wire termination or connector-to-board termination	20 mΩ Max change from baseline
Dielectric Withstanding Voltage	EIA-364-20 Method B 300 VDC minimum for 1 minute Applied voltage may be product / application specific	No defect or breakdown between adjacent contacts -AND- 1 mA Max Leakage Current

Notes:
1. If the durability requirement on the connector is greater than that of the module, modules may be replaced after their specified durability rating.
2. The first low level contact resistance reading in each test sequence is used to determine a baseline measurement. Subsequent measurements in each sequence are measured against this baseline.

Table 16 describes the testing procedures necessary to validate performance criteria not validated by EIA-364-1000 testing. The tests are to be performed in such a way that the parameters/ requirements defined in Table 14 are met.

Table 16- Additional Test Procedures

Tests	Test Descriptions and Details	Pass/ Fail Criteria
Mechanical/ Physical Tests		
Mating Force[1]	EIA-364-13 To be tested with cage, connector, and module. Latching mechanism deactivated (locked out).	Refer to Table 14 -AND- No physical damage to any components
Unmating Force[1]		
Latch Retention[1]	EIA-364-13 To be tested with cage, connector, and module. Latching mechanism engaged (not locked out).	
Latch Strength	An axial load applied using a static load or ramped loading to the specified load. To be tested with cage, connector, and module or module representative tool without heat sinks Latching mechanism engaged (not locked out).	
Cage Retention to Host Board	Tested with module, module analog, or fixtures mated to cage. Pull cage in a direction perpendicular to the board at a rate of 25.4mm/min to the specified force.	No physical damage to any components -AND- Cage shall not separate from board
Electrical Tests		
Current	EIA-364-70 Method 3, 30-degree temperature rise Contacts energized: All signal and power contacts energized simultaneously	Refer to Table 14 for current magnitude

Note:
1. Values listed in Table 14 apply with or without the presence of a riding heat sink.

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